SERVICE MANUAL

COMPACT DISC PLAYER

SANSUI PC-V750

(Silver & Black Model)

CAUTION

1. Parts identified by the ⚠ symbol on the schematic diagram and the parts list are critical for safety. Use only replacement parts that have critical characteristics recommended by the manufacturer.
2. Make leakage-current or resistance measurements to determine that exposed parts are acceptably insulated from the supply circuit before returning the appliance to the customer.

Sansui

SANSUI ELECTRIC CO., LTD.

• SPECIFICATIONS

Type	Compact disc digital audio system
Optical pick-up	3-beam laser
Error correction	CIRC
D/A conversion	16 bit linear
Frequency response	5 Hz~20 kHz +0.5/−0.5 dB
Harmonic distortion	Less than 0.003% (1 kHz)
Signal-to-noise ratio	100 dB (IEC-A-WTD)
Dynamic range	Better than 95 dB
Wow and Flutter	Below measurable limits
Channel separation	Better than 90 dB (1 kHz)
Output voltage	2 V
Power requirements	110~120V/220~240V (50/60 Hz)
For U.S.A. and Canada	120V (60 Hz)
Power consumption	14 watts
Dimensions	430 mm (16-15/16")W 82 mm (3-7/32")H 308.5 mm (12-5/23")D
Weight	4.8 kg (10.7 lbs) net

- Design and specifications subject to changes without notice for improvements.

CAUTION

1. The symbols, UL, CSA, SA, BS, UK, EU, AS and XX on the parts list and the schematic diagram mean followings respectively.

   UL .... Manufactured for U.S.A market.
   (Underwriters Laboratories approved model.)
   CSA .... Manufactured for Canadian market.
   SA .... Manufactured for South African market.
   BS, UK .... Manufactured for United Kingdom market.
   EU .... Manufactured for European market.
   AS .... Manufactured for Australian market.
   XX .... Standard Version.
   NON MARK ..... Common Parts.

2. Some printed circuit boards are not supplied as the assembled. To separate these in this service manual, the stock No's are not indicated at the ends of the board names. However, the individual parts on the circuit boards are provided by orders.

3. Since some of capacitors and resistors are omitted from parts lists in this service manual, refer to the Common Parts List for capacitors & resistors, which was issued on February 1983.

4. Abbreviations in this service manual are as follows.

- Abbreviations List

C.R.	: Carbon Resistor	E.B.L.	: Low Leak Bi-Polar Electrolytic Capacitor
S.R.	: Solid Resistor	Ta.C.	: Tantalum Capacitor
Ce.R	: Cement Resistor	F.C.	: Film Capacitor
M.R.	: Metal Film Resistor	M.P.	: Metalized Paper Capacitor
F.R.	: Fusing Resistor	P.C.	: Polystyrene Capacitor
N.I.R.	: Non-Inflammable Resistor	G.C.	: Gimmic Capacitor
A.R.	: Array Resistor	A.C.	: Array Capacitor
C.C.	: Ceramic Capacitor	V.R.	: Variable Resistor
C.T.	: Ceramic Capacitor, Temperature Compensation	S.V.R.	: Semi Variable Resistor
E.C.	: Electrolytic Capacitor	SW.	: Switch
E.L.	: Low Leak Electrolytic Capacitor	Chip R.	: Chip Resistor
E.B.	: Bi-Polar Electrolytic Capacitor	Chip C.	: Chip Capacitor

Cautions concerning handling of the laser

This unit uses a laser beam, which can be quite dangerous when viewed directly at its source. Please be sure to observe the following cautions.

A. Position of protection unit and of the adjustment volume.

1. The bonnet and clamper form a cabinet to protect the operator from laser light. Thus, removing the bonnet and raising the clamper lever (Refer to Fig. B) may cause the inoidence of laser light from the convex lens. This laser light will be directly on the eye.
2. The volume for the adjustment of the laser output is R112 of the mechanism APC circuit board (Refer to Fig. A).
   Turning R112 clockwise will increase the level of the laser power output.

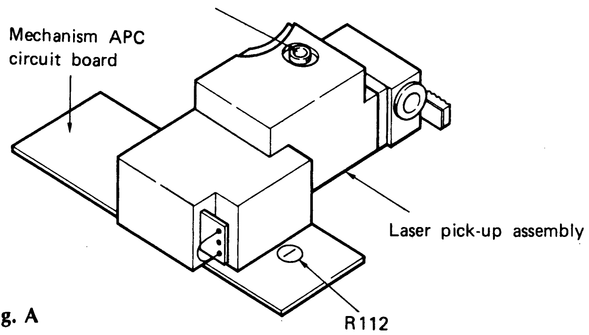


Fig. A

B. Interlocking switch for laser beam.

The laser beam will be output when the following conditions have been satisfied and the laser interlocking switch S101 of the mechanism circuit board NO. S101 is activated when the disc tray is retracted.

1 With the AC power switch ON, the laser beam will be output for three seconds when the disc tray is in the retracted position.

2 When the disc tray is in the extended position, turn on the AC power switch. The disc tray will be retracted, and the laser beam will be output for three seconds.

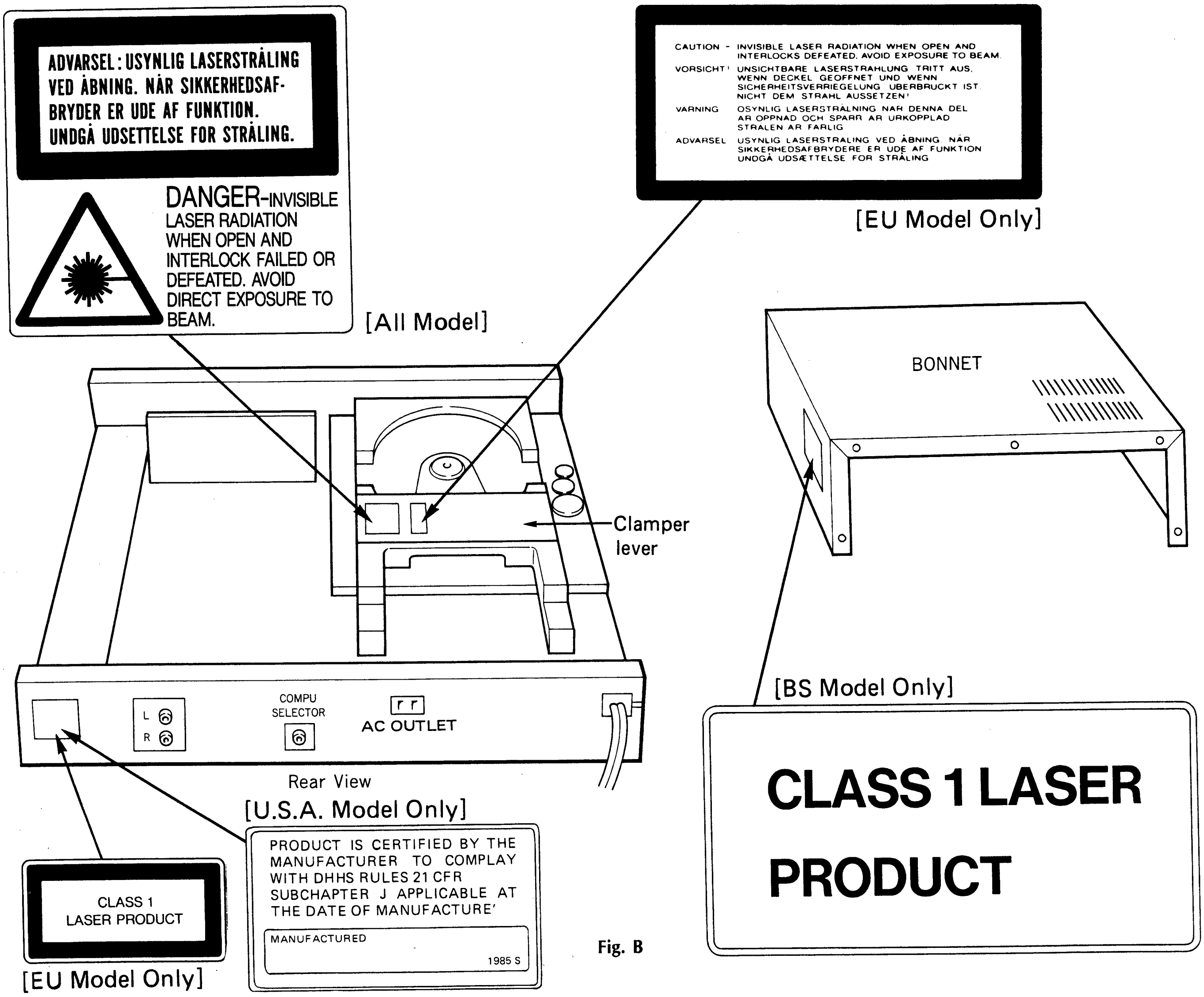
3 With a disc in position, once the counter display sets itself to 0000 after the lead-in track has been read, press the PLAY switch and the laser beam will be output. If there is no disc in the tray, the laser beam will be output for 18 seconds after the PLAY switch has been pressed.

C. Cautionary points to minimize danger.

1 Since the laser beam is extremely dangerous when viewed directly at its source, do not look directly at the laser pick-up assembly when the laser beam is being output. Additionally, even when viewing the laser beam only, be sure that your are at least 30cm away from it when it is in operation.

2 When the laser beam is in operation, do not bring any part of your body into direct contact with or inclose proximity to the convex lens.

D. The following label has been affixed to the unit, listing the proper procedure for working with the laser beam.



ADVARSEL: USYNLIG LASERSTRÅLING VED ÅBNING. NÅR SIKKERHEDSAF-BRYDER ER UDE AF FUNKTION. UNDGÅ UDSETTELSE FOR STRÅLING.

DANGER-INVISIBLE LASER RADIATION WHEN OPEN AND INTERLOCK FAILED OR DEFEATED. AVOID DIRECT EXPOSURE TO BEAM.

CAUTION - INVISIBLE LASER RADIATION WHEN OPEN AND INTERLOCKS DEFEATED. AVOID EXPOSURE TO BEAM.

VORSICHT' UNSICHTBARE LASERSTRAHLUNG TRITT AUS, WENN DECKEL GEOFFNET UND WENN SICHERHEITSVERRIEGELUNG UBERBRUCKT IST. NICHT DEM STRAHL AUSSETZEN'

VARNING OSYNLIG LASERSTRÅLNING NAR DENNA DEL AR OPPNAD OCH SPARR AR URKOPPLAD STRÅLEN AR FARLIG

ADVARSEL USYNLIG LASERSTRALING VED ÅBNING. NÄR SIKKERHEDSAFBRYDERE ER UDE AF FUNKTION UNDGÅ UDSÆTTELSE FOR STRÅLING

CLASS 1 LASER PRODUCT

PRODUCT IS CERTIFIED BY THE MANUFACTURER TO COMPLAY WITH DHHS RULES 21 CFR SUBCHAPTER J APPLICABLE AT THE DATE OF MANUFACTURE'

MANUFACTURED

1985 S

CLASS 1 LASER PRODUCT

Fig. B

Denna CD-spelare innehåller en laser som avger laserstrålning överstigände gräsen för laserklass 1.

1. ADJUSTMENTS

NOTES ON ADJUSTMENT AND PRELIMINARY PROCEDURES

1. Turn the power off and remove the bonnet.
2. Refer to the parts location on Page 19 for the adjustment point.
3. Use the YEDS-7 test disc.
4. Carry out preliminary procedures in the following order:

1) Rotate the Loading mechanism gear S_1 and pull the disc tray out.

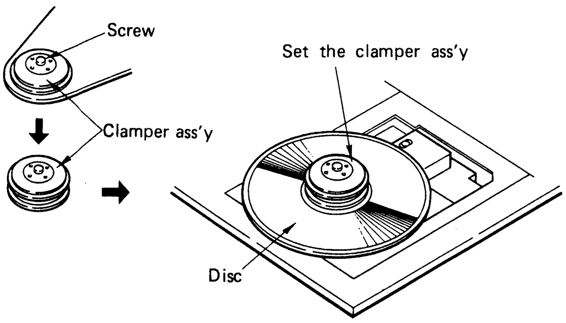
2) When the disc tray is fully extended, lift the clamper lever vertically.

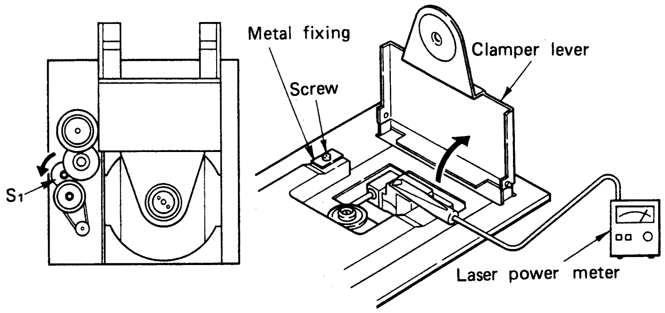
3) Remove the disc tray's metal fixing and, then pull the disc tray out.

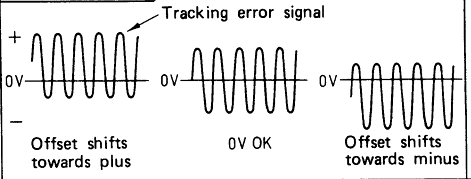
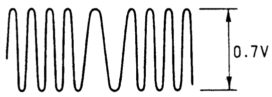
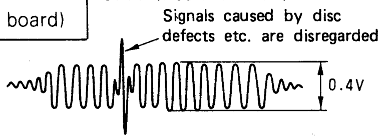
4) Remove the screw of the clamper assembly attached to the clamper lever and remove the clamper assembly.

5) Use a screw to assemble the clampers which had been slid off vertically and use it as a jig.

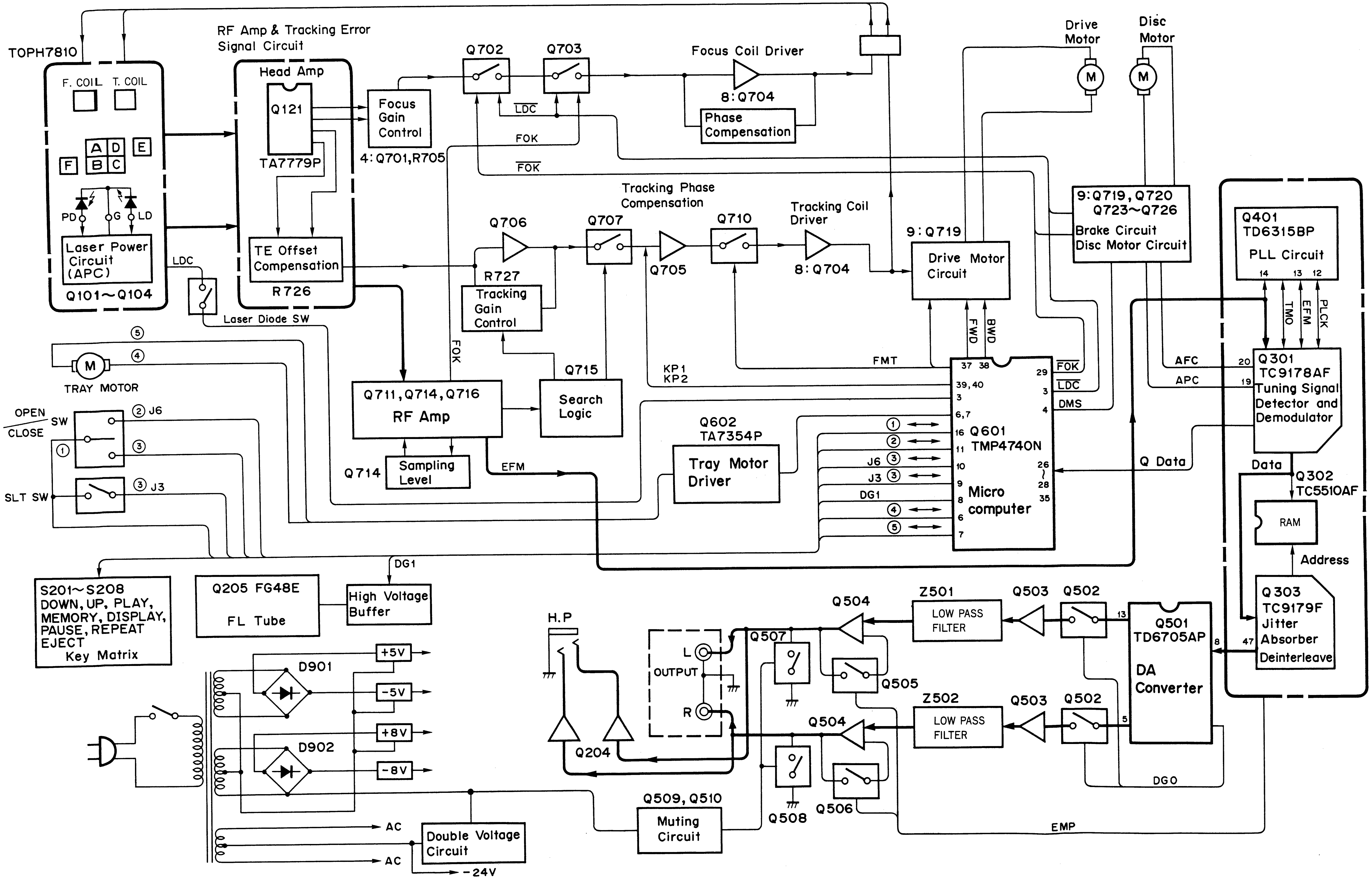
* For your protection, do not look directly at the laser pickup or allow your eyes to get near it while performing adjustments.





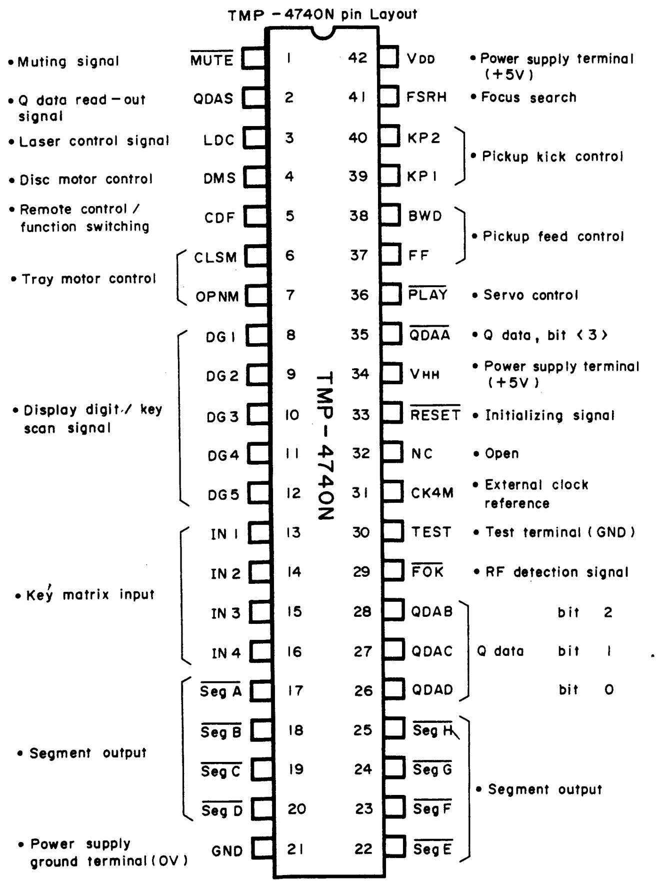
	Adjustment	Point of Measurement	Point of Adjustment	Content of Adjustment	Conditions for Adjustment
1	Pickup Laser Power Adjustment (Rough Adjustment After Replacement)	Upper surface of the pick-up lens power meter (do not touch the sensor part on the lens surface)	R112 (mechanism APC board)	270μW	1. Power switch ... OFF 2. Rotate the mechanism PC board fully counter-clockwise. 3. Disconnect the main board's JW164. 4. Remove the short pin for pickup laser diode protection. 5. Turn the power switch ON and perform the adjustment. 6. After adjustment, turn the power switch OFF and connect the JW164.
2	Focus Balance Adjustment	Connect oscilloscope between TP9 (RF) and TP16 (GND) (AC range 0.2V/DIV, 0.5μsec/DIV)	R112 (mechanism APC board)	Set RF oscillation to maximum.	1. Remove the crank lever, place YEDS-7 test disc in position, and use the removed clampers to hold it. 2. Turn the power switch ON and play the test disc on track No.30.
3	Fine Adjustment of Laser Power	Same as above	R112 (mechanism APC board)	1.0V (Peak to Peak)	Same as above
4	Tracking Error Offset Adjustment	Connect oscilloscope between TP5 (GND) and TP6 (Tracking error signal) (DC range 0.2V/DIV, 0.5msec/DIV)	R27 (mechanism board)	DC 0V 	1. Play YEDS-7 track No.11 (Play is not possible if R726 is far off) 2. Disconnect JW197 (feed motor) 3. Disconnect JW168 (tracking) (Be sure to disconnect JW197 first) 4. Keep in this condition for the following adjustment (5)
5	Tracking, Gain Adjustment	Same as above	R727 (main board)	0.7V (Peak to Peak) 	1. In the condition described above, make the main board's R705 and R727 the mechanical center. 2. After adjustments 5 and 6, turn the power switch OFF and connect the main board's JW197 and JW168.
6	Focus gain signal	TP5 (GND), TP2 (focus error signal)	R705 (main board)	0.4V (Peak to Peak) 	
7	Analog Output Offset Adjustment	Connect DC voltmeter between TP13(L-CH), TP12(R-CH), and TP17(GND).	R507(L-CH), R508(R-CH), (main board)	DC 0V ± 10mV	1. Power switch ... ON 2. Do not set disc.

2. BLOCK DIAGRAM


TOPH7810
F. COIL
T. COIL
A D
B C
E
F
PD
G
LD
Laser Power Circuit (APC)
Q101～Q104
LDC
Laser Diode SW
RF Amp & Tracking Error Signal Circuit
Head Amp
Q121
TA7779P
TE Offset Compensation
R726
Focus Gain Control
4:Q701,R705
Q702
Q703
LDC
FOK
FOK
Focus Coil Driver
8:Q704
Phase Compensation
Drive Motor
Disc Motor
M
M
Tracking Phase Compensation
Q706
Q707
Q710
Q705
Tracking Coil Driver
8:Q704
R727
Tracking Gain Control
9:Q719
Drive Motor Circuit
9:Q719,Q720
Q723～Q726
Brake Circuit
Disc Motor Circuit
Q401
TD6315BP
PLL Circuit
14 13 12
TMO
EFM
PLCK
FWD
BWD
FOK
Q715
Search Logic
KP1
KP2
FMT
Q711,Q714,Q716
RF Amp
Q714
Sampling Level
EFM
⑤
④
TRAY MOTOR
OPEN
CLOSE
SW
② J6
③
①
SLT SW
③ J3
Q602
TA7354P
Tray Motor Driver
① ② J6 ③ J3 ③ DG1 ④ ⑤
Q601
TMP4740N
Micro computer
37 38 29 3 4 39,40 3 6,7 16 11 10 9 8 6 7 26 ～ 28 35
FOK
LDC
DMS
AFC
APC
20
19
Q301
TC9178AF
Tuning Signal Detector and Demodulator
Q Data
Data
Q302
TC5510AF
RAM
Address
Q303
TC9179F
Jitter Absorber Deinterleave
47
8
DG1
S201～S208
DOWN, UP, PLAY, MEMORY, DISPLAY, PAUSE, REPEAT
EJECT
Key Matrix
Q205 FG48E
FL Tube
High Voltage Buffer
D901
D902
+5V
-5V
+8V
-8V
AC
AC
Double Voltage Circuit
-24V
H.P
Q204
OUTPUT
L
R
Q507
Q508
Q509, Q510
Muting Circuit
Q504
Q505
Q504
Q506
Z501
LOW PASS FILTER
Z502
LOW PASS FILTER
Q503
Q502
Q503
Q502
13
5
Q501
TD6705AP
DA Converter
DGO
EMP

3. INTERIOR BLOCK DIAGRAM & TERMINAL FUNCTION OF IC

TMP-4740N (Microcomputer IC)

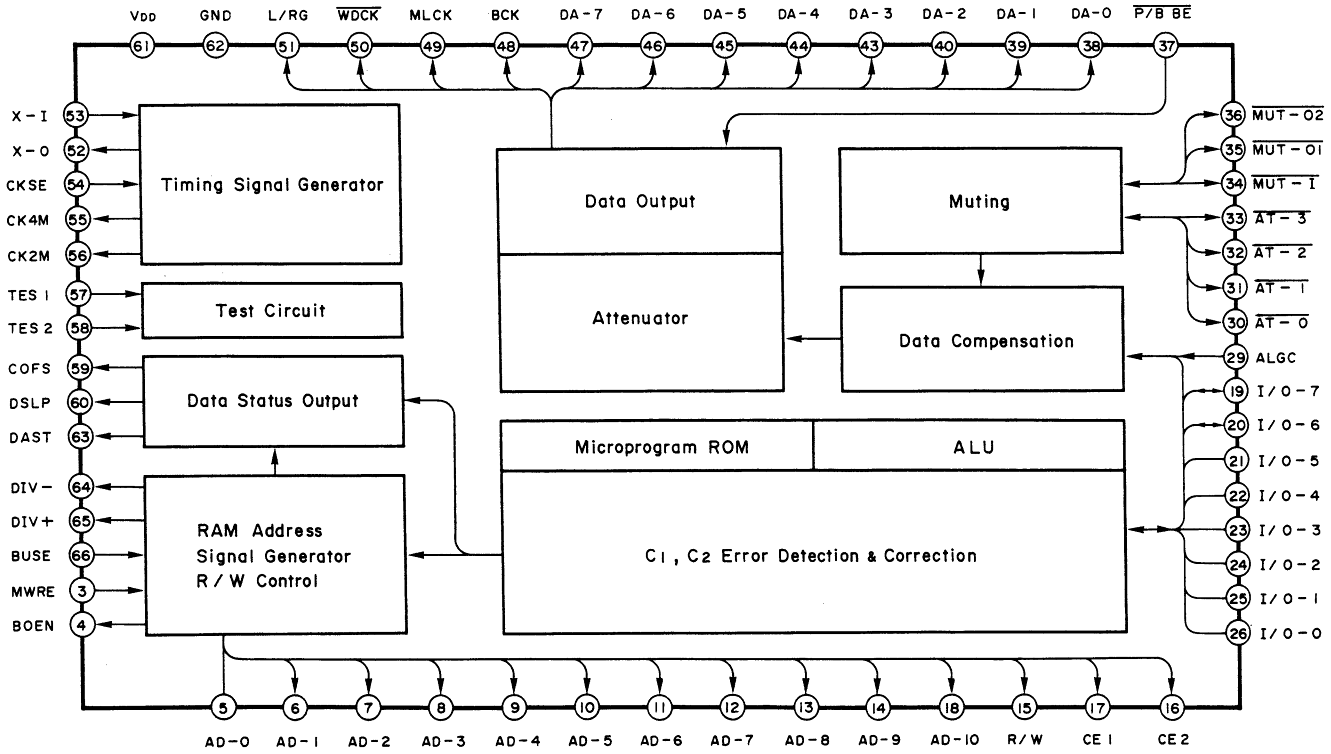

TMP -4740N pin Layout
TMP-4740N
• Muting signal
MUTE 1
• Q data read-out signal
QDAS 2
• Laser control signal
LDC 3
• Disc motor control
DMS 4
• Remote control / function switching
CDF 5
• Tray motor control
CLSM 6
OPNM 7
• Display digit / key scan signal
DG1 8
DG2 9
DG3 10
DG4 11
DG5 12
• Key matrix input
IN1 13
IN2 14
IN3 15
IN4 16
• Segment output
Seg A 17
Seg B 18
Seg C 19
Seg D 20
• Power supply ground terminal (OV)
GND 21
42 VDD • Power supply terminal (+5V)
41 FSRH • Focus search
40 KP2
39 KP1
• Pickup kick control
38 BWD
37 FF
• Pickup feed control
36 PLAY • Servo control
35 QDAA • Q data, bit ‹3›
34 VHH • Power supply terminal (+5V)
33 RESET • Initializing signal
32 NC • Open
31 CK4M • External clock reference
30 TEST • Test terminal (GND)
29 FOK • RF detection signal
28 QDAB
27 QDAC
26 QDAD
Q data bit 2
bit 1
bit 0
25 Seg H
24 Seg G
23 Seg F
22 Seg E
• Segment output

Pin No.	Port Designation		Signal Code	I/O	Initial Status	Function
26	K0	K00	QDAD	I	*	"Q data/error status" data input.
27		K01	QDAC	I	*	"Q data/error status" data input.
28		K02	QDAB	I	*	"Q data/error status" data input.
29		K03	$\overline{\text{FOK}}$	I	*	RF detection signal input. "L" when RF signal present.
35	R8	R80	$\overline{\text{QDAA}}$	I	*	1. "Q data read-out possible" signal input. 2. Q data input.
36		R81	$\overline{\text{PLAY}}$	O	H	Servo control signal. "L": Servo ON.
37		R82	FF	O	L	Pickup motor control. At "H", pickup is moved towards the outside of the disc.
38		R83	BWD	O	L	Pickup motor control. At "H", pickup is moved towards the inside of the disc.
39	R9	R90	KP1	O	L	Pickup motor control. At "H", forward kick is performed.
40		R91	KP2	O	L	Pickup motor control. At "H", backward kick is performed.
41		R92	FSRH	O	L	Focus search signal. When LDC is "H", a 1-Hz pulse is supplied.

Terminal Functions 〔TMP-4740N〕

Pin No.	Port Designation		Signal Code	I/O	Initial Status	Function
1	R4	R40	$\overline{\text{MUTE}}$	O	L	Muting is ON when muting output is "L". Terminal is "H" only during play, "L" in all other modes.
2		R41	QDAS	O	L	1. Q data/error status detection signal. 2. Q data read-out signal.
3		R42	LDC	O	L	Laser control signal. Laser is OFF when at "L", ON when at "H"
4		R43	DMS	O	L	Disc motor control signal. Motor stops when at "L".
5	R5	R50	CDF	I/O	H/L	Depending on switch position in key matrix, two functions are selected: 1. Data input for wired remote control. 2. Function switching output.
6		R51	CLSM	O	H	Tray motor control signal. "L" during tray opening process.
7		R52	$\overline{\text{O}}$PNM	O	H	Tray motor control signal. "L" during tray closing process.
8		R53	DG1	O	L	Display digit selection signal. Selection at "H".
9	R6	R60	DG2	O	L	1. Display digit selection signal. 2. Scan signal for key matrix.
10		R61	DG3	O	L	1. Display digit selection signal. 2. Scan signal for key matrix.
11		R62	DG4	O	L	1. Display digit selection signal. 2. Scan signal for key matrix.
12		R63	DG5	O	L	1. Display digit selection signal. 2. Scan signal for key matrix.
13	R7	R70	IN1	I	*	Key matrix input.
14		R71	IN2	I	*	Key matrix input.
15		R72	IN3	I	*	Key matrix input.
16		R73	IN4	I	*	Key matrix input.
17	P1	P10	$\overline{\text{Seg A}}$	O	H	Display segment data output. "L": ON. (1) segment a (2) colon
18		P11	$\overline{\text{Seg B}}$	O	H	Display segment data output. "L": ON. (1) segment b (2) PAUSE indicator
19		P12	$\overline{\text{Seg C}}$	O	H	Display segment data output. "L": ON. (1) segment c
20		P13	$\overline{\text{Seg D}}$	O	H	Display segment data output. "L": ON. (1) segment d (2) REPEAT indicator
22	P2	P20	$\overline{\text{Seg E}}$	O	H	Display segment data output. "L": ON. (1) segment e (2) TNO indicator
23		P21	$\overline{\text{Seg F}}$	O	H	Display segment data output. "L": ON. (1) segment f (2) LAP indicator
24		P22	$\overline{\text{Seg G}}$	O	H	Display segment data output. "L": ON. (1) segment g (2) REM indicator
25		P23	$\overline{\text{Seg H}}$	O	H	Display segment data output. "L": ON. (1) MEMORY indicator
21		Vss	GND			Power supply ground (0 V)
30		TEST	TEST	I		Test mode setting input. To be connected to ground.
31		XIN	CK4M	I		External clock reference input.
32		XOUT		O		Open
33		$\overline{\text{RESET}}$	$\overline{\text{RESET}}$	I		Initializing signal input. Initializing is effected at "L".
34		VHH	VHH			Memory backup power supply. To be connected to VDD.
42		VDD	VDD			Power supply (+5V)

TC-9179F (Jitter Absorption & Deinterleaving IC)


VDD 61
GND 62
L/RG 51
WDCK 50
MLCK 49
BCK 48
DA-7 47
DA-6 46
DA-5 45
DA-4 44
DA-3 43
DA-2 40
DA-1 39
DA-0 38
P/B BE 37
X-I 53
X-O 52
CKSE 54
CK4M 55
CK2M 56
TES 1 57
TES 2 58
COFS 59
DSLP 60
DAST 63
DIV- 64
DIV+ 65
BUSE 66
MWRE 3
BOEN 4
Timing Signal Generator
Test Circuit
Data Status Output
RAM Address Signal Generator R / W Control
Data Output
Attenuator
Muting
Data Compensation
Microprogram ROM
ALU
C1, C2 Error Detection & Correction
36 MUT-02
35 MUT-01
34 MUT-I
33 AT-3
32 AT-2
31 AT-1
30 AT-0
29 ALGC
19 I/O-7
20 I/O-6
21 I/O-5
22 I/O-4
23 I/O-3
24 I/O-2
25 I/O-1
26 I/O-0
5 AD-0
6 AD-1
7 AD-2
8 AD-3
9 AD-4
10 AD-5
11 AD-6
12 AD-7
13 AD-8
14 AD-9
18 AD-10
15 R/W
17 CE1
16 CE2

Terminal Functions 〔TC-9179F〕

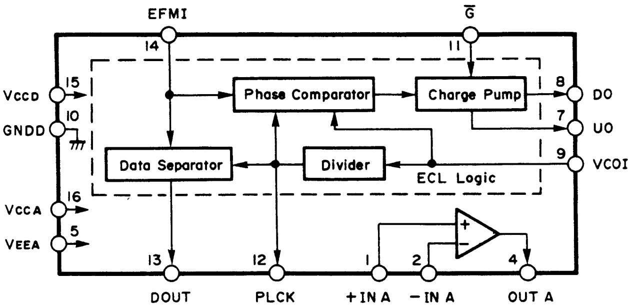
Pin No.	Signal Code	I/O	Function
27, 61	VDD	—	Power supply
28, 62, 67	VSS	—	Ground
2	PBFS	I	Frame synchronization input. Accepts symbol data period signals for each frame supplied by TC9178F. * Connected to PBFS (pin 56) of TC9178F.
3	MWRE	I	Memory write request input. Accepts MWRE signal supplied by TC9178F. * Connected to MWRE (pin 67) of TC9178F.
4	BOEN	O	Output enable terminal. Supplies a control signal to set the symbol data outputs (DBO0 ~ DBO7) to ON when MWRE signal from TC9178F can be accepted. * Connected to BOEN (pin 66) of TC9178F.
5 ~ 14 18	AD-0 ~ AD-9 AD-10	O	RAM address signal terminal. Supplies address control signal for external RAM (8-bit x 2kW). Connected to external RAM address terminal.
15	R/W	O	Read/write signal terminal. Controls read/write function of external RAM. Connected to external RAM R/W terminal. "H": Read, "L": Write.
16	CE2	O	Chip enable 2 output terminal. When C_2 correction data are written to external RAM, this terminal becomes active. In normal operation, it is open.
17	CE1	O	Chip enable 1 output terminal. This terminal becomes active when read/write is performed with external RAM. Connected to external RAM $\overline{\text{CE1}}$ terminal.
19 ~ 26	I/O-7 ~ I/O-0	I/O	Data bus. Serves for sending and receiving data to and from external RAM and TC9178F. Connected to external RAM I/O-0 ~ I/O-7 and TC9178F DBO0 ~ DBO7.
29	ALGC	I	C_2 correction processing selector terminal. Serves to select algorithm processing for frames whose error symbol cannot be detected in the C_2 error-correction section. In normal operation, terminal is "L". When at "H", the error symbol detected in C_1 is sent to the compensation circuit instead of C_2

Pin No.	Signal Code	I/O	Function	
30 ~ 33	$\overline{\text{AT-0}}$ ~ $\overline{\text{AT-3}}$	I/O	Digital attenuator terminal. Serves to level monitoring and external control of internal digital attenuator. During $\overline{\text{WDCK}}$ = "L", the terminal serves as output (for monitoring) and during $\overline{\text{WDCK}}$ = "H" as input (for external control).	
34	$\overline{\text{MUT-I}}$	I	Muting control terminal. Serves to automatic control of built-in digital attenuator. At "L", the amount of attenuation increases (output finally becoming digital "0"), at "H", the amount decreases (output moving towards 0 dB).	
35	$\overline{\text{MUT-01}}$	O	Muting 1 output terminal. In case of a burst error of more than 64 frames or jitter absorption buffer overflow, "L" is fed out.	
36	$\overline{\text{MUT-02}}$	O	Muting 2 output terminal. In case of a deinterleaving error for 3 continuous frames, "L" is fed out.	
37	$\overline{\text{P/S SE}}$	I	Parallel/serial data output selector terminal. At "L", output is parallel. At "H", output is serial.	
38	DA-0	O	$\overline{\text{P/S SE}}$ = "L"	$\overline{\text{P/S SE}}$ = "H"
			Output terminal for LSB of 8-bit data.	Serial data output starting with LSB.
39	DA-1	O	Output terminal for 2nd bit after LSB of 8-bit data.	8-bit compensation flag output for MSB.
40	DA-2	O	Output terminal for 3rd bit after LSB of 8-bit data.	8-bit compensation flag output for LSB.
43	DA-3	O	Output terminal for 4th bit after LSB of 8-bit data.	Terminal becomes "H" if MSB level is −30 dB and LSB compensation flag is detected.
44	DA-4	O	Output terminal for 5th bit after LSB of 8-bit data.	CK1M output terminal. Clock signal produced by dividing CK2M by factor 2. (1.058 MHz)

Terminal Functions〔TC-9179F〕

Pin No.	Signal Code	I/O	Function	
			$\overline{\text{P/S SE}}$ = "L"	$\overline{\text{P/S SE}}$ = "H"
45	DA-5	O	Output terminal for 6th bit after LSB of 8-bit data.	Right-channel aperture output terminal.
46	DA-6	O	Output terminal for 7th bit after LSB of 8-bit data.	Left-channel aperture output terminal.
47	DA-7	O	Output terminal for MSB of 8-bit data.	Serial data output starting with MSB.
48	BCK	O	Bit clock output terminal. Used when feeding out serial data. Output starts in sync with falling clock pulse. (1.4112 MHz)	
49	MLCK	O	MSB/LSB clock output terminal. Generated by dividing BCK by factor 8. Used as set clock for 8-bit parallel output. (176.4 kHz)	
50	$\overline{\text{WDCK}}$	O	Word clock output terminal. Generated by dividing BCK by factor 16. Used to define output length for 1 word. (88.2 kHz)	
51	L/RG	O	Sampling frequency output terminal. Produced by dividing $\overline{\text{WDCK}}$ by factor 2. Used to define left-channel/right-channel data output. "L": left channel, "H": right channel.	
52	X-O	O	Quartz connection terminals. Serve to connect the quartz for clock frequency generation. (with integrated feedback resistor and amplifier)	
53	X-I	I		
54	CKSE	I	Clock select terminal. Serves to select the quartz frequency. "H" or open signifies 8.4672 MHz, "L" signifies 4.2336 MHz. (With integrated pull-up resistor)	
55	CK4M	O	4-MHz clock output terminal, supplying 4.2336 MHz. Can also be used as microcomputer clock.	
56	CK2M	O	2-MHz clock output terminal, supplying 2.1168 MHz. Used as clock output for TC9178F. Connected to C21K (pin 7) of TC9178F.	
57	TES1	I	Test terminals (with pull-up resistor). In normal operation, these terminals are "H" or open.	
58	TES2			
59	COFS	O	Frame synchronization terminal for output of correction frame.	
60	DSLP	O	Data status latch signal output terminal.	
63	DAST	O	Data status output terminal. The jitter absorption memory and results of C_1 and C_2 error detection appear in bit-serial form at this terminal. With an external latch circuit, monitoring can be carried out.	
64	DIV-	O	Buffer-up output terminal. When the jitter absorption memory buffer (capacity ±4 frames) has reached either +2 or +3 frames, the terminal becomes "H". This output is fed to DIV- of TC9178F and used to reduce the disc motor revolution speed. • Connected to pin 5 (DIV-) of TC9178F.	
65	DIV+	O	Buffer-down terminal. When the jitter absorption memory buffer (capacity ±4 frames) has reached either −2 or −3 frames, the terminal becomes "H". This output is fed to DIV+ of TC9178F and used to increase the disc motor revolution speed. • Connected to pin 4 (DIV+) of TC9178F.	
66	BUSE	I	Buffer select input terminal. Serve to select the output conditions of DIV−/DIV+. With terminal at "H", output starts from ±2 frames and with terminal at "L" from ±3 frames.	

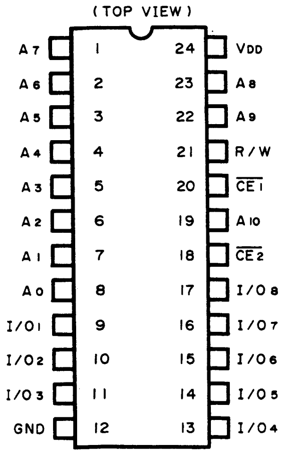
TD6315AP/BP (PLL IC)



Terminal Functions〔TD6315AP/BP〕

Pin No.	Signal Code	Function
1	INA+	Positive input terminal of internal OP amp. Fixed to ≒ 1/2 VCCD potential. Forms guardring for INA- in conjunction with terminal 3 (NC).
2	INA−	Negative input terminal of internal OP amp. The output signals UO and DO of the internal charge pump and the resistance-added signal from the TMO terminal of TC9178F are fed in here.
3	NC	Non-connected terminal at same potential as INA+. Serves to isolate the INA− and OUTA terminals.
4	OUTA	Output terminal of internal OP amp. The connection to INA− via capacitor C and resistor R forms a laglead type filter, supplying the input voltage for the VCO.
5	VEEA	Analog power supply, negative terminal.
6	NC	Non-connected terminal at same potential as INA+. Serves to isolate the VEEA and UO, DO terminals.
7	UO	Charge pump-up signal output terminal. If the rising edge of the PLCK signal (VCO frequency signal divided by 4) is delayed in comparison to the edge of the supplied EFMI signal, the "L" level output period becomes longer and the VCO frequency is increased. In-phase clock condition: "L" = 1/2 PLCK. • Except during the "L" cycle, the terminal is at high-impedance.
8	DO	Charge pump-down signal output terminal. If the rising edge of the PLCK signal(VCO frequency signal divided by 4) is leading in comparison to the edge of the supplied EFMI signal, the "H" level output period becomes longer and the VCO frequency is decreased. In-phase clock condition: "H" = 1/2 PLCK. • Except during the "H" cylce, the terminal is at high-impedance.
9	VCOI	VCO input/output terminal. An AC-coupled signal is fed in here via a capacitor.
10	GNDD	Digital Power supply, ground terminal.
11	$\overline{\text{G}}$	Input terminal used to set the charge pump outputs UO and DO to high-impedance. By making this terminal "L", the outputs are set to high-impedance and the VCO frequency is in the hold condition. (TTL level)
12	PLCK	Clock output teminal used for data separation. This clock signal is produced in the PLL circuit from the EFMI input, by dividing the VCO frequency (17.3 MHz) by the factor 4. Connected to the PLCK terminal of the C^2-MOS processor TC9178F. 4.32 MHz, duty cycle 50%.
13	DOUT	EFMI signal output teminal. The signal is synchronized with the rising edge of the PLCK signal. Connected to the EFMI terminal of the C^2-MOS processor TC9178F.
14	EFMI	Input terminal for digital EFMI signal, derived by passing the RF signal from the disc through a data slicer. (TTL level)
15	VCCD	Digital power supply terminal.
16	CCCA	Analog power supply terminal.

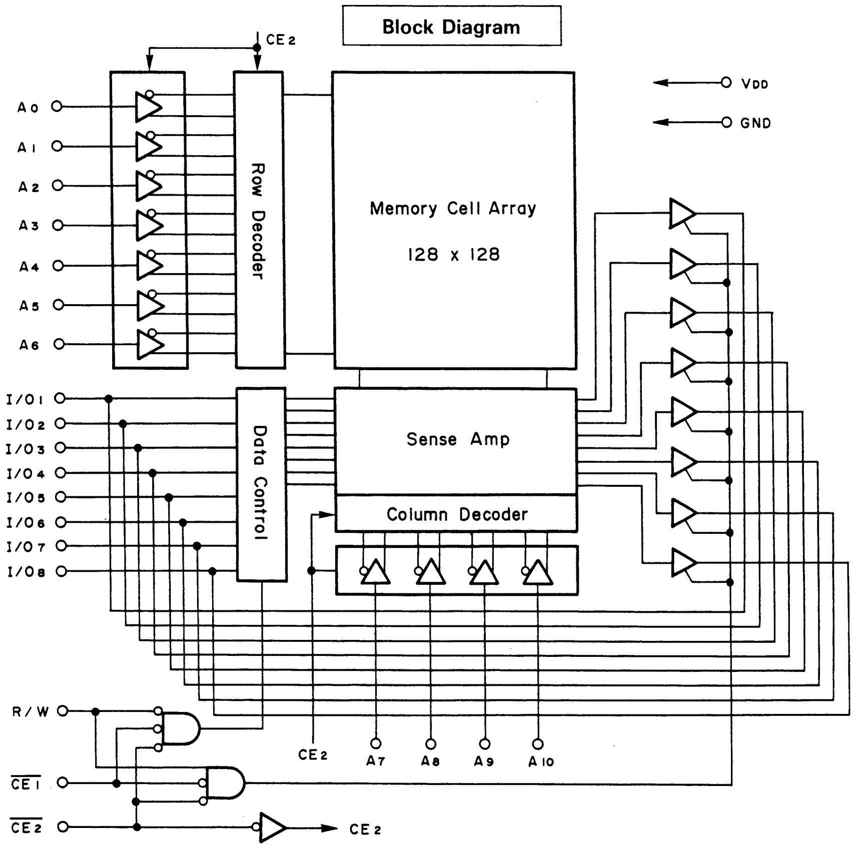
TC-5516AF (2048 Word x 8 Bit Static RAM IC)


(TOP VIEW)
A7 1
A6 2
A5 3
A4 4
A3 5
A2 6
A1 7
A0 8
I/O1 9
I/O2 10
I/O3 11
GND 12
24 VDD
23 A8
22 A9
21 R/W
20 $\overline{CE_1}$
19 A10
18 $\overline{CE_2}$
17 I/O8
16 I/O7
15 I/O6
14 I/O5
13 I/O4

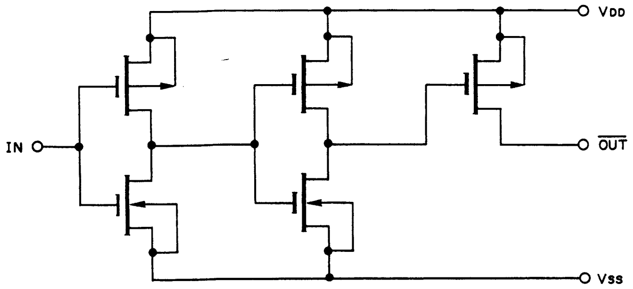
Pin Designation

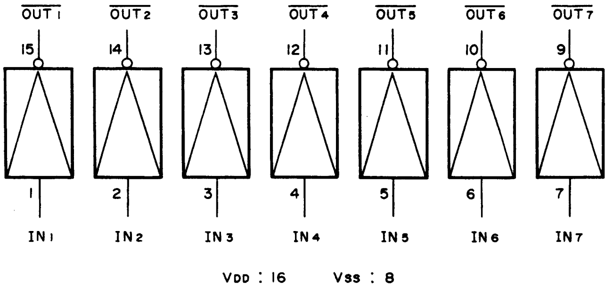
A_0 ~ A_{10}	Address input
R/W	Read/Write input
$\overline{CE_1}$, $\overline{CE_2}$	Chip Enabel Input
I/O_1 ~ I/O_8	Data input/Output
VDD/GND	Power Supply

Block Diagram

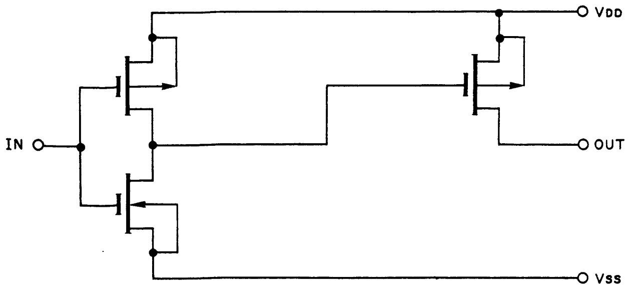

CE2
VDD
GND
A0
A1
A2
A3
A4
A5
A6
Row Decoder
Memory Cell Array
128 x 128
I/O1
I/O2
I/O3
I/O4
I/O5
I/O6
I/O7
I/O8
Data Control
Sense Amp
Column Decoder
R/W
$\overline{CE1}$
$\overline{CE2}$
CE2
A7
A8
A9
A10
CE2

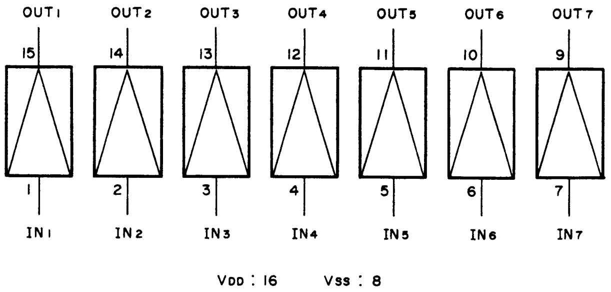
TC-5067BP (Buffer Amp IC)


VDD
IN
$\overline{OUT}$
Vss


$\overline{OUT1}$
$\overline{OUT2}$
$\overline{OUT3}$
$\overline{OUT4}$
$\overline{OUT5}$
$\overline{OUT6}$
$\overline{OUT7}$
15
14
13
12
11
10
9
1
2
3
4
5
6
7
IN1
IN2
IN3
IN4
IN5
IN6
IN7
VDD : 16 Vss : 8

TC-5066BP (Buffer Amp IC)


VDD
IN
OUT
Vss

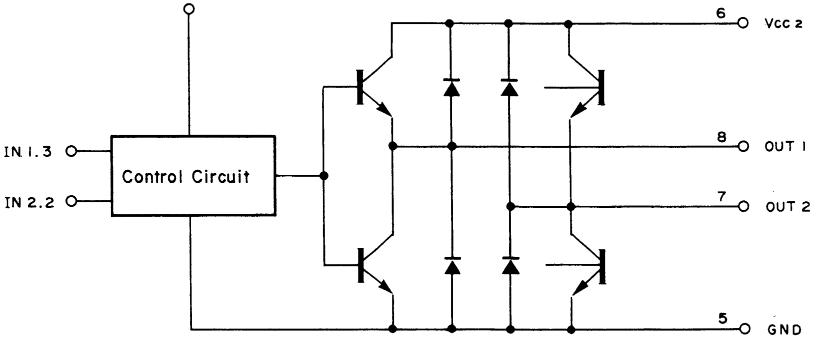

OUT1
OUT2
OUT3
OUT4
OUT5
OUT6
OUT7
15
14
13
12
11
10
9
1
2
3
4
5
6
7
IN1
IN2
IN3
IN4
IN5
IN6
IN7
VDD : 16 Vss : 8

TA-7354P (Driver IC for Motor-Direction Inversion Switching)

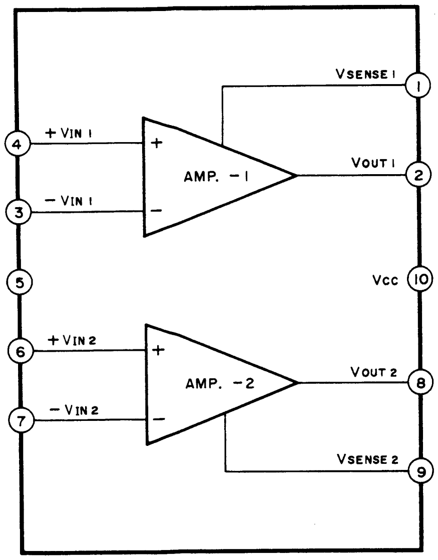
Pin Designation

IN 1	IN 2	OUT 1	OUT 2
1	1	L	L
0	1	L	H
1	0	H	L
0	0	High-impedance	High-impedance

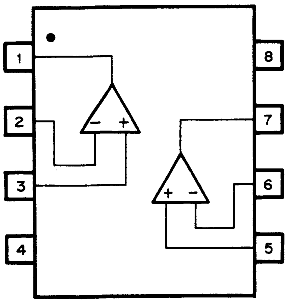
Block Diagram


Vcc 1
6 Vcc 2
8 OUT 1
7 OUT 2
5 GND
IN 1.3
IN 2.2
Control Circuit

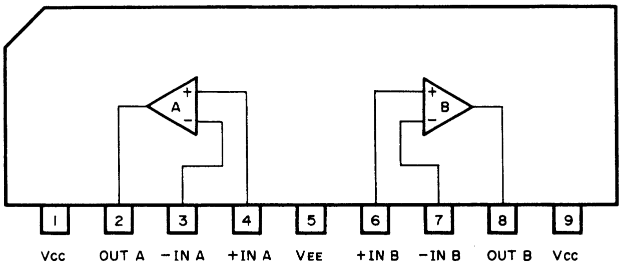
TA-7256P (OP Amp IC)


VSENSE 1
1
+VIN 1
4
VOUT 1
2
AMP. −1
−VIN 1
3
5
Vcc
10
+VIN 2
6
VOUT 2
8
AMP. −2
−VIN 2
7
VSENSE 2
9

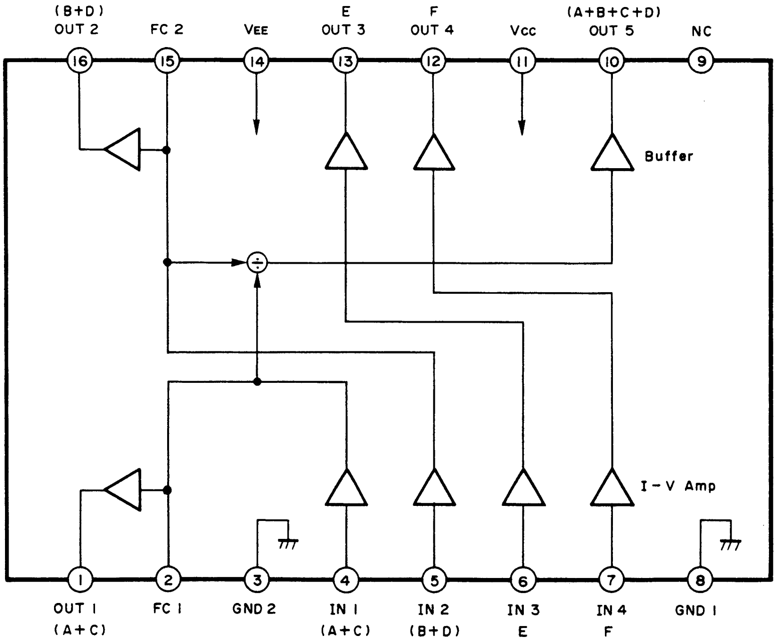
NJM-5532D (OP Amp IC)



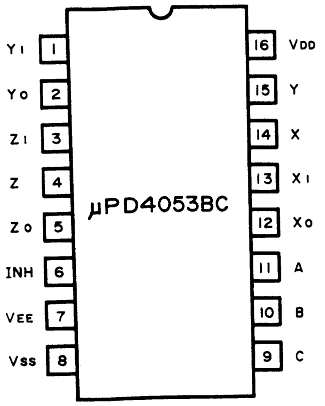
TA-75458S (OP Amp IC)


A
B
1
2
3
4
5
6
7
8
9
Vcc
OUT A
−IN A
+IN A
VEE
+IN B
−IN B
OUT B
Vcc

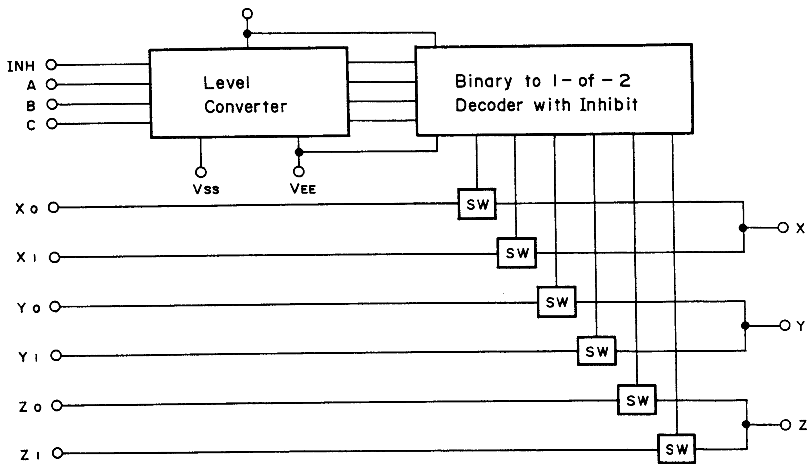
TA-7779P (Head-Amp IC for Laser-Receiving Photodiode)


(B+D) OUT 2
16
FC 2
15
VEE
14
E OUT 3
13
F OUT 4
12
Vcc
11
(A+B+C+D) OUT 5
10
NC
9
Buffer
I−V Amp
1
OUT 1 (A+C)
2
FC 1
3
GND 2
4
IN 1 (A+C)
5
IN 2 (B+D)
6
IN 3 E
7
IN 4 F
8
GND 1

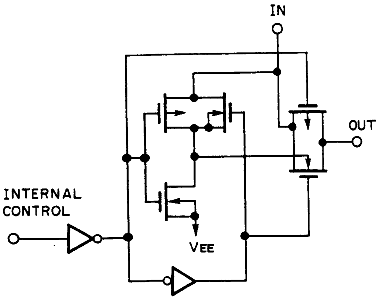
μPD-4053BC (Analog Switching IC)


Y1 1
Y0 2
Z1 3
Z 4
Z0 5
INH 6
VEE 7
Vss 8
16 VDD
15 Y
14 X
13 X1
12 X0
11 A
10 B
9 C
μPD4053BC

Block Diagram


VDD
INH
A
B
C
Level Converter
Binary to 1-of-2 Decoder with Inhibit
Vss
VEE
X0
X1
Y0
Y1
Z0
Z1
SW
X
Y
Z

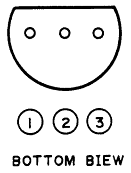
Equivalent Circuit of Analog Switching Section

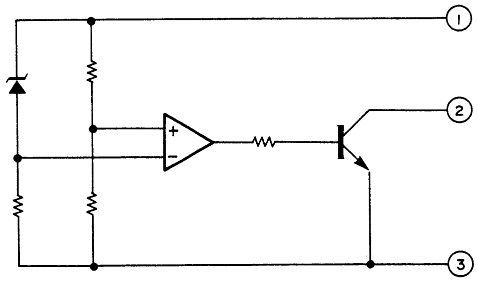

IN
OUT
INTERNAL CONTROL
VEE

Truth Table

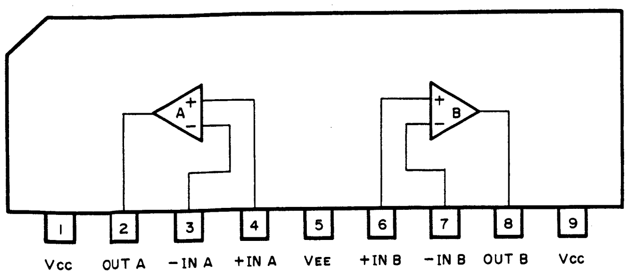
Control Input				"ON" Channel
INHIBIT	C	B	A	μPD4053BC
L	L	L	L	Z0. Y0. X0
L	L	L	H	Z0. Y0. X1
L	L	H	L	Z0. Y1. X0
L	L	H	H	Z0. Y1. X1
L	H	L	L	Z1. Y0. X0
L	H	L	H	Z1. Y0. X1
L	H	H	L	Z1. Y1. X0
L	H	H	H	Z1. Y1. X1
H	x	x	x	NONE

PST-520D (Low-Power System Reset IC)

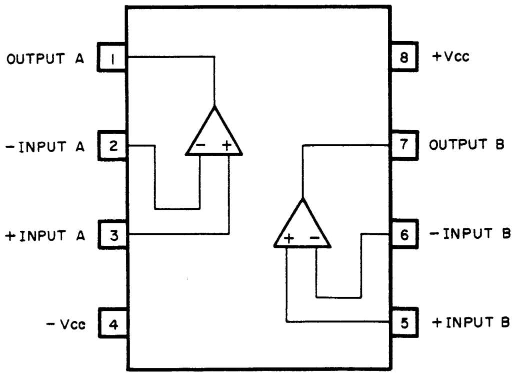

① ② ③
BOTTOM BIEW



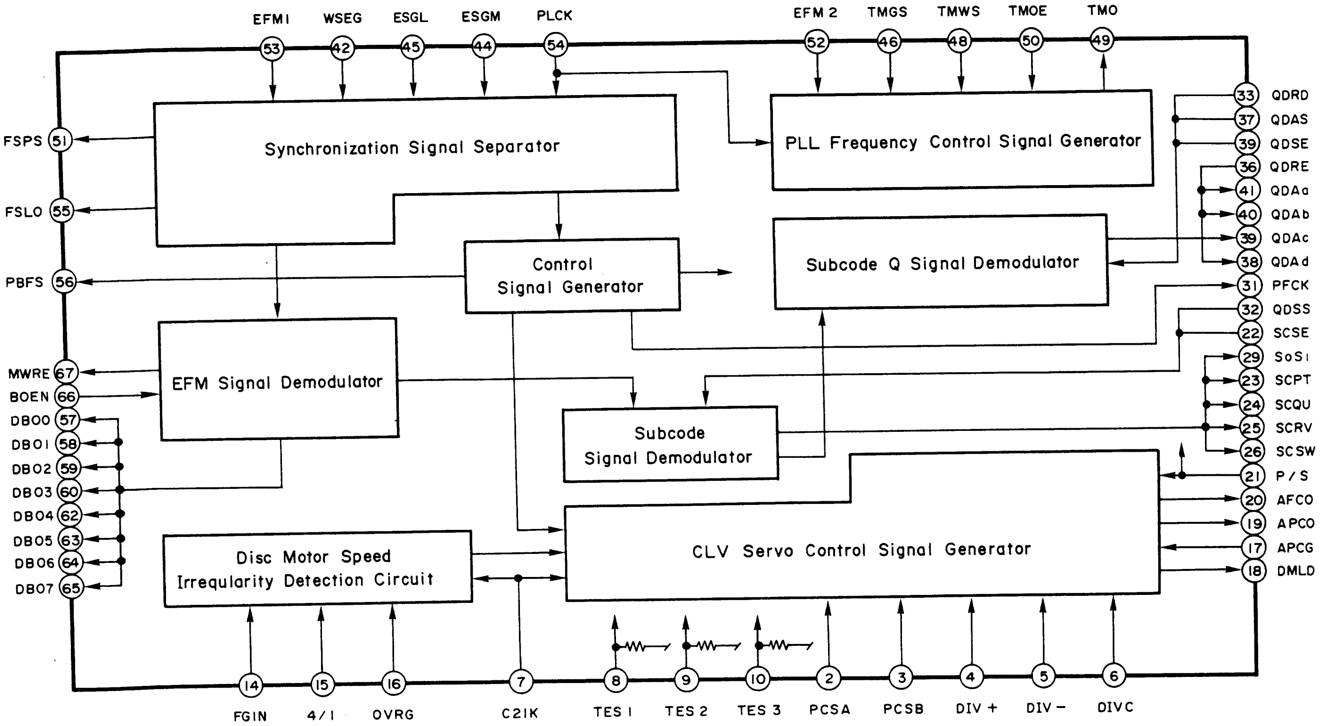
TA-75557S (OP Amp IC)


A
B
1 Vcc
2 OUT A
3 −IN A
4 +IN A
5 VEE
6 +IN B
7 −IN B
8 OUT B
9 Vcc

NJM-072D-E (OP Amp IC)


OUTPUT A 1
−INPUT A 2
+INPUT A 3
−Vcc 4
8 +Vcc
7 OUTPUT B
6 −INPUT B
5 +INPUT B

TC-9178F (Sync Signal Detection & Demodulator IC)


EFMI
WSEG
ESGL
ESGM
PLCK
EFM 2
TMGS
TMWS
TMOE
TMO
53
42
45
44
54
52
46
48
50
49
Synchronization Signal Separator
PLL Frequency Control Signal Generator
Control Signal Generator
Subcode Q Signal Demodulator
EFM Signal Demodulator
Subcode Signal Demodulator
CLV Servo Control Signal Generator
Disc Motor Speed Irregularity Detection Circuit
FSPS 51
FSLO 55
PBFS 56
MWRE 67
BOEN 66
DB00 57
DB01 58
DB02 59
DB03 60
DB04 62
DB05 63
DB06 64
DB07 65
33 QDRD
37 QDAS
39 QDSE
36 QDRE
41 QDAa
40 QDAb
39 QDAc
38 QDAd
31 PFCK
32 QDSS
22 SCSE
29 SoSı
23 SCPT
24 SCQU
25 SCRV
26 SCSW
21 P/S
20 AFCO
19 APCO
17 APCG
18 DMLD
14 FGIN
15 4/1
16 OVRG
7 C2IK
8 TES 1
9 TES 2
10 TES 3
2 PCSA
3 PCSB
4 DIV +
5 DIV −
6 DIVC

Terminal Functions 〔TC-9178F〕

<table>
<tr><th>Pin No.</th><th>Signal Code</th><th>I/O</th><th>Function</th></tr>
<tr><td>1</td><td>NC</td><td>—</td><td>Non-connected terminal.</td></tr>
<tr><td>2
3</td><td>PCSA
PCSB</td><td>I</td><td>Terminal used to select the phase comparator frequency of the APC signal for CLV servo control.
Phase comparator frequency fc = 7.35 kHz (frame synchronization signal)/N
<table>
<tr><th>PCSA</th><th>PCSB</th><th>N</th><th>f_C(Hz)</th></tr>
<tr><td>L</td><td>L</td><td>6</td><td>1225</td></tr>
<tr><td>H</td><td>L</td><td>8</td><td>918.75</td></tr>
<tr><td>L</td><td>H</td><td>12</td><td>612.5</td></tr>
<tr><td>H</td><td>H</td><td>16</td><td>459.375</td></tr>
</table></td></tr>
<tr><td>4
5
6</td><td>DIV+
DIV−
DIVC</td><td>I</td><td>Input terminal used to set the phase comparison reference frequency in the APC signal generator (for CLV servo control) to "variable". A buffer memory status signal is fed to this terminal from TC9179F.The amount of frequency variation is determined by the DIVC terminal.
<table>
<tr><th>DIV+</th><th>DIV−</th><th>DIVC</th><th>Reference frequency ratio</th><th>Disc motor speed</th></tr>
<tr><td>L</td><td>L</td><td>*</td><td>1/288</td><td></td></tr>
<tr><td>H</td><td>L</td><td>L</td><td>1/287.5</td><td>increases</td></tr>
<tr><td>H</td><td>L</td><td>H</td><td>1/287</td><td>increases</td></tr>
<tr><td>L</td><td>H</td><td>L</td><td>1/288.5</td><td>decreases</td></tr>
<tr><td>L</td><td>H</td><td>H</td><td>1/289</td><td>decreases</td></tr>
<tr><td>H</td><td>H</td><td>*</td><td>1/288</td><td></td></tr>
</table>
*: either level.
* Connected to DIV+ (pin 65) and DIV− (pin 64) of TC-9179F.</td></tr>
<tr><td>7</td><td>C21K</td><td>I</td><td>Input terminal for 2.1168 MHz signal. Duty cycle = 50%. The frequency is produced by dividing the quartz reference frequency fed in from TC-9179F (8.4672 MHz) by the factor 4.
* Connected to CK2M (pin 56) of TC-9179F.</td></tr>
<tr><td>8~
10</td><td>TES1~
TES3</td><td>I</td><td>Test input terminal. In ordinary operation, the terminal is "H" or open. (With pull-up resistor)</td></tr>
</table>

<table>
<tr><th>Pin No.</th><th>Signal Code</th><th>I/O</th><th>Function</th></tr>
<tr><td>11</td><td>NC</td><td>—</td><td>Non-connected terminal.</td></tr>
<tr><td>12</td><td>EMPH</td><td>O</td><td>Terminal used for determination of emphasis status (by control bit of subcode Q). At "H", de-emphasis is switched ON.</td></tr>
<tr><td>13</td><td>2/4S</td><td>O</td><td>Terminal for determination of 2-channel/4-channel status (by control bit of subcode Q).
"L": 2-channel, "H": 4-channel.</td></tr>
<tr><td>14</td><td>FGIN</td><td>I</td><td>Input terminal for FG pulse from disc motor. 1 or 4 FG pulse are fed to this terminal for each motor revolution, and AFC/APC output is controlled to keep motor speed within the 175 ~ 740 rpm range.
<table>
<tr><th>Disc motor speed (rpm)</th><th>AFCO</th><th>APCO</th></tr>
<tr><td>~175</td><td>Fixed to "H"</td><td>Duty cycle 50%, output fixed.</td></tr>
<tr><td>175~740</td><td>Reguler operation</td><td>Regular operation</td></tr>
<tr><td>740~</td><td>Fixed to "L"</td><td>Duty cycle 50%, output fixed.</td></tr>
</table></td></tr>
<tr><td>15</td><td>4/1</td><td>I</td><td>Terminal used to set the FG input signal to 1 or 4 pulses per revolution.
<table>
<tr><th>FG pulse</th><th>4/1</th></tr>
<tr><td>1</td><td>H</td></tr>
<tr><td>4</td><td>L</td></tr>
</table></td></tr>
<tr><td>16</td><td>OVRG</td><td>I</td><td>Terminal used to determine whether disc motor speed control is to be performed via FGIN input or not.
At "H", FGIN is active.</td></tr>
<tr><td>17</td><td>APCG</td><td>I</td><td>Input terminal for ON/OFF switching of the APC signal generator for CLV servo control.
"L" (generator OFF):
APC output is set to phase difference "0", i.e. duty cycle is fixed to 50%. At the same time, the internal phase comparator reference frequency generator is set to phase difference "0" with the compared frequency, therefore phase comparison starts at "0" when the generator is set to ON.
"H" (generator ON):
A PWM signal corresponding to the detected phase difference in regard to the reference frequency is fed out from APC.</td></tr>
</table>

Terminal Functions [TC-9178F]

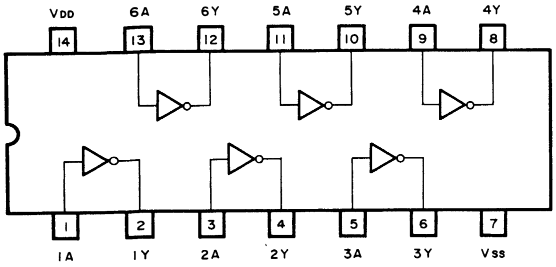
<table>
<tr><th>Pin No.</th><th>Signal Code</th><th>I/O</th><th>Function</th></tr>
<tr><td>18</td><td>DMLD</td><td>O</td><td>Output terminal for disc motor lock detection. This terminal belongs to the AFC signal generator for CLV servo control. The output is a flip-flop signal which is set when the detected frame synchronization frequency is within ±5% and reset if it is more than ±10%. The "set" flip-flop output is "H". This signal is connected to the APCG and serves to control the APC block.</td></tr>
<tr><td>19</td><td>APCO</td><td>O</td><td>APC signal output terminal for CLV servo control. The output is a PWM signal with 8-bit resolution, transmitting frequency of 8.27 kHz, and linear output range of $8\pi/9$.</td></tr>
<tr><td>20</td><td>AFCO</td><td>O</td><td>AFC signal output terminal for CLV servo control. The output is a PWM signal with 8-bit resolution, transmitting frequency of 8.27 kHz, and linear output range of ±10%.</td></tr>
<tr><td>21</td><td>P/S</td><td>I</td><td>Input terminal for ON/OFF switching of CLV servo control signal. During Play, the level is "H", and during Stop it is "L". This input is given priority in the CLV servo control section. If it is "L", the AFC output is also "L", and the duty cycle of the APC output is fixed at 50%.</td></tr>
<tr><td>22</td><td>SCSE</td><td>I</td><td>This terminal serves to determine which set of subcode data is supplied at the 4 terminals SCP/T ~ SCS/W. At "L", the data bits P, Q, R, S and at "H", the data bits T, U, V, W appear at the output.</td></tr>
<tr><td>23
24
25
26</td><td>SC P/T
SC Q/U
SC R/V
SC S/W</td><td>O</td><td>These 4 terminals serve for output of the 8 subcode data bits P, Q, R, S, T, U, V, W. The data are supplied for each frame in 4-bit blocks, selected by the SCSE signal. The frame data switching is synchronized with the falling edge of the PFCK signal.</td></tr>
<tr><td>27
61</td><td>VDD</td><td>—</td><td>Power supply terminals.</td></tr>
<tr><td>28</td><td>VSS</td><td>—</td><td>Ground terminal.</td></tr>
<tr><td>29</td><td>S_0S_1</td><td>O</td><td>Output terminal which becomes "H" during the frame input period when S_0 or S_1 was detected in the subcode synchronization pattern.</td></tr>
<tr><td>30</td><td>NC</td><td>—</td><td>Non-connected terminal.</td></tr>
<tr><td>31</td><td>PFCK</td><td>O</td><td>Output for frame duty cycle ≒ 50%. Subcode data switching is performed in synchronization with the falling edge of this signal.</td></tr>
<tr><td>32</td><td>QDSS</td><td>I</td><td>Terminal for selection of synchronization pattern detection mode used for subcode Q signal demodulation.</td></tr>
<tr><td>33</td><td>QDRD</td><td>I</td><td>This terminal serves for read-out of subcode Q data in 4-bit blocks from terminals QDAa ~ QDAd. When QDRD becomes "H", the 4-bit data to be sent out next are set at terminals QDAa ~ QDAd for an optional period starting with the rising edge of QDRD.
Data read-out can be performed only while the QDRE terminal is "H". When QDRE is "L", the QDRD signal is not accepted. If input of more than 1ck every four frames is not given, QDRE becomes "L".</td></tr>
<tr><td>34~
35</td><td>NC</td><td></td><td>Non-connected terminals.</td></tr>
<tr><td>36</td><td>QDRE</td><td>O</td><td>This output terminal serves to enable subcode Q signal read-out. After error determination of the subcode Q signal (80-bit data) is completed, the block of 4 bits starting with the MSB is set at terminals QDAa ~ QDAd, and the QDRE output level becomes "H". When this terminal is "H", read-out is enabled. If 20 pulses are fed to the QDRD terminal or if the next block of Q data is written before read-out of data from the internal RAM was performed, the terminal becomes "L" and data read-out is disabled.</td></tr>
<tr><td>37</td><td>QDAS</td><td>I</td><td>This terminal serves for switching the subcode Q data output terminals QDAa ~ QDAd.
In order to ensure easy interfacing with the microprocessor, the subcode Q block error check result and the outputs of QDRE and QDAa ~ QDAd are switched by this terminal.
<table>
<tr><th>Terminal designation
QDAS</th><th>QDAa</th><th>QDAb</th><th>QDAc</th><th>QDAd</th></tr>
<tr><td>L</td><td>QDRE</td><td>QDEa</td><td>QDEb</td><td>L</td></tr>
<tr><td>H</td><td>QDAa</td><td>QDAb</td><td>QDAc</td><td>QDAd</td></tr>
</table></td></tr>
</table>

<table>
<tr><th>Pin No.</th><th>Signal Code</th><th>I/O</th><th>Function</th></tr>
<tr><td>38~
41</td><td>QDAa~
d</td><td>O</td><td>The 80-bit subcode Q data, the result of block error determination of these data, and the QDRE signal appear at the respective terminals, depending on the "L" or "H" status of the QDAS terminal. For data transmission to the microprocessor, first QDAS is set to "L" and the Q data error check results are sent. Next, by setting QDAS to "H" and feeding QDRD as input, the Q data are sent consecutively in 4-bit blocks. The terminals QDAa ~ QDAd are three-state terminals which are switched between the output mode and the inpedance mode by the "L" or "H" status of QDSE.
<table>
<tr><th>QDEa</th><th>QDEb</th><th>Check result</th><th>Output data processing</th></tr>
<tr><td>H</td><td>H</td><td>No error</td><td>Direct output</td></tr>
<tr><td>L</td><td>H</td><td>CRCC 1-bit error</td><td>Direct output</td></tr>
<tr><td>H</td><td>L</td><td>Q data 1-bit error</td><td>1-bit correction output</td></tr>
<tr><td>L</td><td>L</td><td>2-bit error or more</td><td>Direct output</td></tr>
</table></td></tr>
<tr><td>42</td><td>WSEG</td><td>I</td><td>Gate signal window selection terminal, used to determine whether the internal synchronization signal is to be used when an EFM signal frame synchronization pattern was detected.
<table>
<tr><th>WSEG</th><th>Gate signal window (PLCK clock counts)</th></tr>
<tr><td>L</td><td>±3</td></tr>
<tr><td>H</td><td>±7</td></tr>
</table></td></tr>
<tr><td>43</td><td>TMWS</td><td>I</td><td>Tmax detection is performed with the EFM signal fed in from EFM2. This terminal permits selection of N for Tmax = N (PLCK).
<table>
<tr><th>TMWS</th><th>N (PLCK)</th></tr>
<tr><td>L</td><td>11±1</td></tr>
<tr><td>H</td><td>11±05</td></tr>
</table>
For explanation of Tmax, refer to paragraph 6 of the following description of operation principles.</td></tr>
<tr><td>44
45</td><td>ESGM
ESGL</td><td>I</td><td>If the frame synchronization pattern is not detected continuously for N frames within the window of the gate signal for protection of the frame synchronization separation, system synchronization is performed via the next frame synchronization pattern outside the window. These two terminals serve for the selection of N.
<table>
<tr><th>ESGL</th><th>ESGM</th><th>N (frames)</th></tr>
<tr><td>L</td><td>L</td><td>12</td></tr>
<tr><td>H</td><td>L</td><td>8</td></tr>
<tr><td>L</td><td>H</td><td>4</td></tr>
<tr><td>H</td><td>H</td><td>2</td></tr>
</table></td></tr>
<tr><td>46</td><td>TMGS</td><td>I</td><td>To prevent errors in Tmax detection, the Tmax value is accepted after it has been detected N times continuously. This terminal serves for the selection of N.
<table>
<tr><th>TMGS</th><th>N</th></tr>
<tr><td>L</td><td>7</td></tr>
<tr><td>H</td><td>4</td></tr>
</table></td></tr>
<tr><td>47</td><td>NC</td><td>—</td><td>Non-connected terminal.</td></tr>
<tr><td>48</td><td>TMO</td><td>O</td><td>The frequency information gained from Tmax detection of the EFM signal fed in from EFM2 is compared to the frequency of PLCK, and the results appear at this three-state terminal. This output can be used as frequency data for the PLL circuit. If the P/S signal is "L" (Stop mode), TMO forcedly becomes "H".
<table>
<tr><th>EFM signal frequency information</th><th>TMO</th></tr>
<tr><td>$f_{Tmax} > f_{PLCK}$</td><td>L</td></tr>
<tr><td>$f_{Tmax} \fallingdotseq f_{PLCK}$</td><td>High-impedance</td></tr>
<tr><td>$f_{Tmax} < f_{PLCK}$</td><td>H</td></tr>
</table></td></tr>
</table>

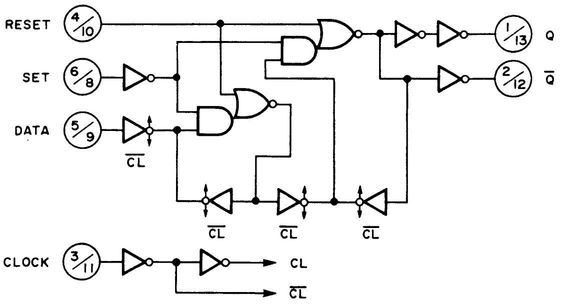
Terminal Functions 〔TC-9178F〕

Pin No.	Signal Code	I/O	Function
49	QDSE	I	Input terminal used to forcedly set the outputs QDAa ~ QDAd to high-impedance. This is achieved when the terminal is "L". This terminal permits effective use of the microprocessor's input ports.
50	TMOE	I	Input terminal used to forcedly set the TMO output to high-impedance. Ordinarily connected to FSPS or FSLO.
51	FSPS	O	Output terminal used to indicate that the system is synchronized by means of the frame synchronization pattern. Depending on the selection of the two inputs ESGL and ESGM, if the frame synchronization pattern cannot be obtained within the gate signal window of N frames, the terminal becomes "H".
52	EFM2	I	Input terminal for the EFM signal obtained from disc playback. The signal from the RF amp is sliced in the level comparator and fed in directly to this input (not synchronized with PLCK).
53	EFMI	I	Input terminal for the EFM signal obtained from disc playback. As opposed to EFM2, the signal fed into this input is synchronized by phase-locking it to the rising edge of the PLCK signal in a PLL circuit.
54	PLCK	I	Input terminal for the clock pulse generated in an external PLL circuit based on HF signal data from disc playback. This input is used for frame synchronization separation and data separation. As system clock, the frequency is 4.32 MHz. Duty cycle is 50%.
55	FSLO	O	When all systems are synchronized by the frame synchronization pattern, i.e. the input patterns exactly match the frame synchronization pattern of the internal frame counter (one frame cycle is always 588 PLCK), then this output terminal becomes "L".
56	PBFS	O	If all frame synchronization signals are "H", the demodulated data U_0 ~ U_{31} are sent to TC-9179F. When this terminal has become "H", the MWRE signal is sent out first, indicating that the U_0 symbol is ready to be fed out externally. * Connected to PBFS (pin 2) of TC-9179F.
57 ~ 60 62 ~ 65	DB00 ~ DB07	I	Output terminals for the demodulated data of the 32 symbols U_0 ~ U_{31} of each frame. These are three-state terminals. When the BOEN input is "L", data are fed out externally. DB00 (LSB) ..... DB07 (MSB) * Connected to I/O-0 ~ I/O-7 of TC-9179F.
66	BOEN	I	Input terminal for the enable signal to set the bus driver for DB00 ~ DB07 to ON. Connected to the BOEN terminal of TC-9179F.
67	MWRE	O	Output terminal for a signal indicating whether the output of DB00 ~ DB07 is ready to be written to an external RAM. When the DB00 ~ DB07 data is set in the transmission register, this terminal becomes "L". When the BOEN signal changes from "H" to "L", the terminal becomes "H". After the PBFS signal has become "H", output is performed 32 times every 17 PLCK pulses. * Connected to MWRE (pin 2) of TC-9179F.

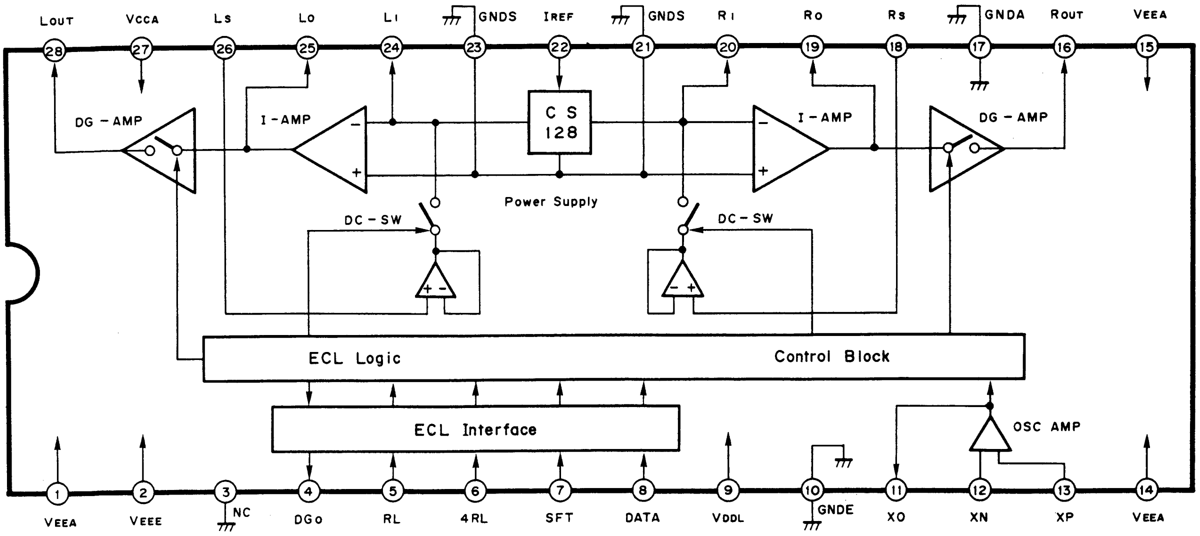
TC-40H004 (Inverter IC)


VDD
6A
6Y
5A
5Y
4A
4Y
14
13
12
11
10
9
8
1
2
3
4
5
6
7
1A
1Y
2A
2Y
3A
3Y
Vss

1/2 TC-4013BP/BF (Flip-flop IC)


RESET
4/10
SET
6/8
DATA
5/9
CL
CL
CL
CL
CLOCK
3/11
CL
CL
1/13
Q
2/12
Q̄

TD-6705AP (D/A Converter IC)


LOUT
VCCA
LS
LO
LI
GNDS
IREF
GNDS
RI
RO
RS
GNDA
ROUT
VEEA
28
27
26
25
24
23
22
21
20
19
18
17
16
15
DG - AMP
I - AMP
C S 128
I - AMP
DG - AMP
Power Supply
DC - SW
DC - SW
ECL Logic
Control Block
ECL Interface
OSC AMP
1
2
3
4
5
6
7
8
9
10
11
12
13
14
VEEA
VEEE
NC
DGO
RL
4RL
SFT
DATA
VDDL
GNDE
XO
XN
XP
VEEA

4. DISASSEMBLY PROCEDURES

(For a description of the parts listed in the following text, refer to the exploded diagram of the mechanism assembly, on page 15.)

1. Replacing the laser pick-up

1 Remove the bonnet.
2 Press the OPEN button, causing the disc tray ⑫ to slide out.
3 Turn off the power.
4 Remove the disc tray stopper ⑩ , and remove the disc tray by pulling it forward.
5 Remove the four screws ㊶ securing the mechanism assembly chassis.
6 Remove the flexible wire Ⓣ (refer to Fig. 4-3) from the mechanism circuit board.
7 Turn the mechanism assembly chassis upside-down.
8 Remove the screw Ⓩ (refer to Fig. 4-3) securing the pick-up assembly, and remove the pick-up assembly from the mechanism assembly chassis.
9 Remove the two screws Ⓤ (refer to Fig. 4-4), and remove the locking gear from the pick-up assembly.
10 Remove the two screws Ⓨ (refer to Fig. 4-3)screwing the mechanism APC circuit board (refer to Fig. 4-4).
NOTE: Never remove screwⒶ(refer to Fig. 4-5).
11 Locate the terminals to which are attached the red and black lead wires connecting the pick-up assembly to the mechanism APC circuit board, and short-circuit the terminals (to prevent parts damage due to high voltage static electricity). Remove the red, black and white lead wires, if the same pick-up unit is to be remounted in its original position again(refer to Fig. 4-1).
12 After remounting the pick-up and re-attaching the connectors and lead wires, remove the shortcircuits from the terminals that were shorted out in the above step 11.
13 When replacing the existing laser pick-up unit with a new unit, attach the lead wires to the connectors, and remove the shorting pin protecting the laser diode(refer to Fig. 4-3).

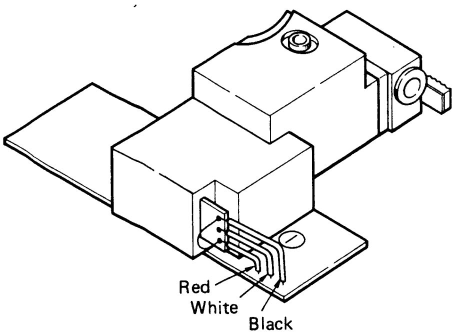


Fig. 4-1

* Before removing the flexible PC board and the lead wires, solder the two terminals together, short-circuiting them.

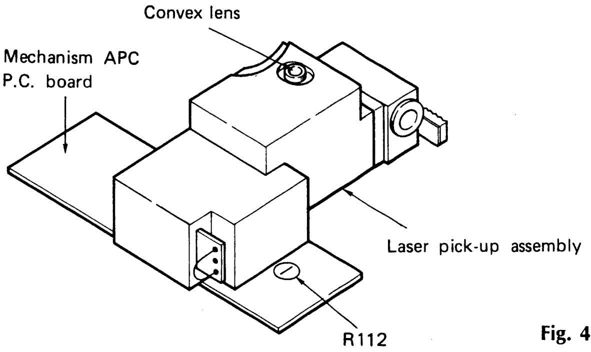


Fig. 4-2

* Short-circuited terminals

Be sure to remove the lead wires after short-circuiting the terminals

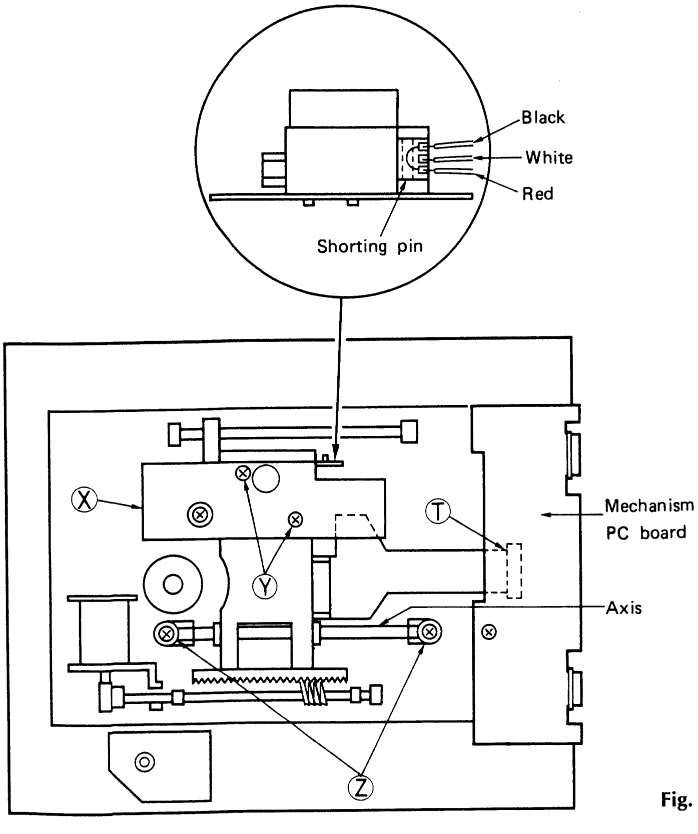


Fig. 4-3

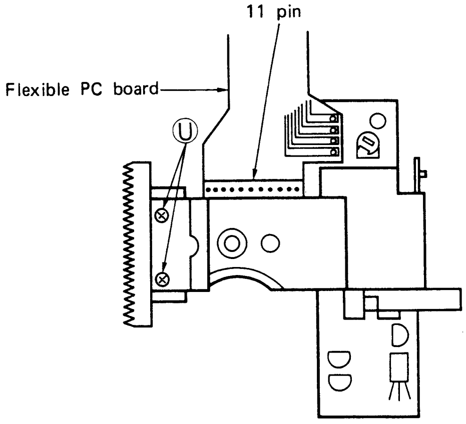


Fig. 4-4

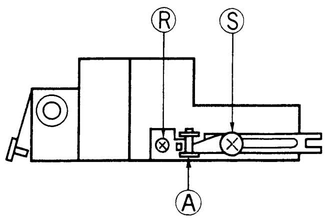


Fig. 4-5

Never remove or move this screw.

* The optical pick-up have been grouped into A and B, with the rank for each pick-up being marked on a label affixed to the side of the pick-up unit, as shown in the figure below. If the ranks of the original pick-up unit and that of the replacement are identicalm there is no need to change the complementary resistor.
If the rank of the replacement pick-up unit is different from that of the original, it will become necessary to replace the existing resistance with a value corresponding to the rank of the replacement pick-up, as shown in the table below.

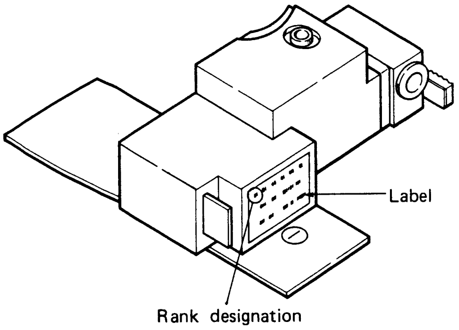

Label
Rank designation

Fig. 4-6

Rank \ Part number	Mechanism APC circuit board R113
B	5.6K
A	Remove

2. Procedure for attaching the cam gear and drive gear

1 When attaching the cam gear and drive gear, align the marking on the cam gear with the circular mark on the drive gear, and insert them together so that the protruding portion of the cam gear comes between the cam links as shown below.

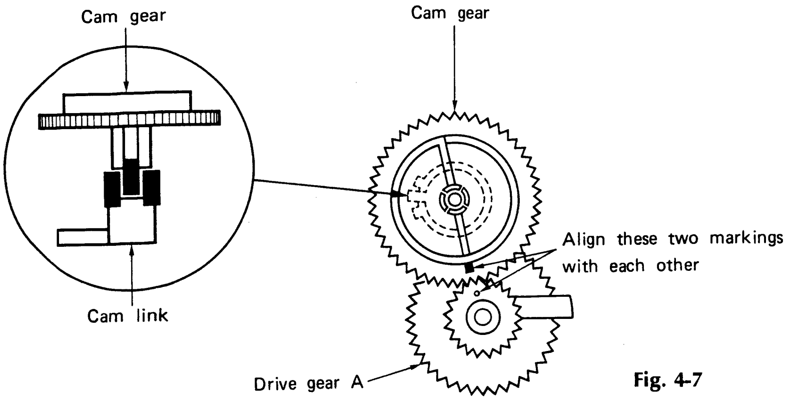

Cam gear
Cam link
Cam gear
Align these two markings
with each other
Drive gear A

Fig. 4-7

3. Procedure for installing the disc tray

Insert the disc tray so that the shaft of the clamper lever and the marking on the cam gear are positioned as shown below. After inserting the disc tray, open the clamper lever, and attach the stopper piece. However, when installing the disc tray after the cam gear and drive gear have been installed, starting from the position shown in Fig. 4-7, rotate drive gear A approximately twice clockwise so that it is positioned as shown in Fig. 4-8, and than carry out the procedure for installing the disc tray.

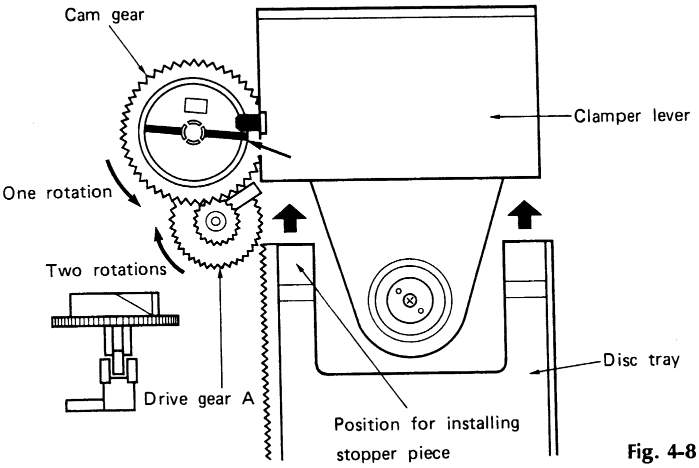

Cam gear
Clamper lever
One rotation
Two rotations
Drive gear A
Disc tray
Position for installing
stopper piece

Fig. 4-8

5. EXPLODED VIEW & PARTS LIST

Exploded View of Mechanism

Parts List

Parts No.	Stock No.	Description
1	58035300	Spring Clamper Lifter
2	————	Clamper Lever Ass'y
3	58075500	Screw, 2×5 B Type
4	58040000	Clamper Plate
5	58039700	Clamper Yoke
6	58039800	Magnet
7	58075600	Magnet Spacer
8	58039900	Clamper
9	58075700	Screw, 2.6×6 B Type
10	58035000	Stopper Plate
11	58039500	Sub Tray
12	58039400	Disc Tray
13	58075800	Spring
14	58039200	Tray Lever
15	58039600	Spring
16	58039300	Tray Slider
17	58075900	Screw, 2.6×6 B Type
18	58039100	Leaf Switch
19	58037800	Cam Gear
20	58038600	Washer, 2.1ϕ
21	58037900	Drive Gear
22	58037500	Drive Gear Ass'y
23	58037700	Loading Gear B
24	58038500	Cam Link
25	58038400	Lift Lever
26	58040300	Screw, 2.6×13 FC Type
27	58076000	Screw, 2.6×10 B Type
28	58038200	Tray Guide
29	58076100	Screw, 2.6×3 B Type
30	58038100	Roller Mount Ass'y
31	58037600	Roller
32	————	Main Chassis
33	58039600	Spring
34	58038000	Motor Spacer
35	58038900	Loading Motor Ass'y
36	————	Mecha Board Ass'y
37	58076200	Washer, 1.7ϕ
38	58076300	T. T. Ring
39	58076400	Clample Spring
40	58076500	Screw, 2.6×5 B Type
41	58076600	Screw, 2.6×8 B Type
42	58035100	Mecha, Spacer A
43	58035200	Cushion
44	————	Mecha Chassis
45	58035400	Mecha Spring A
46	58035500	Mecha Spring B
47	58036300	Motor Mount
48	58036500	Motor Spring
49	58036600	Drive Motor Ass'y
50	58036400	Leaf Switch
51	58076700	Screw, 2×5 B Type
52	58076800	Screw, 2.6×10 BSB Type
53	58036000	Shaft Holder B
54	58035900	Guide Shaft B
55	————	APC Mecha Board
56	58076900	Shaft Holder A
57	58036200	Disc Motor Ass'y
58	58077000	Drive Spring
59	58037300	Drive Shaft Ass'y
60	58037400	Wheel Gear
61	58037200	Rack Gray
62	58077100	Screw, 2×3 B Type
63	58038800	Rack Spring
64	58036100	Flexible Wire Board
67	58038300	Lift Slider
68	58036700	Guide Plate
69	58077200	Screw, 2.6ϕ×4 B Type
70	58037000	Mecha Holder Screw

Parts No.	Stock No.	Description
71	58037100	Pick-up Spring
73	58036800	Guide Lever
74	58077300	Leaf Switch
75	58038700	Drive Belt
76	58077400	Screw, 2×4 B Type
79	58077500	Washer 1.9ϕ
80	58036900	Laser Pick-up

Exploded View of Set

Parts List

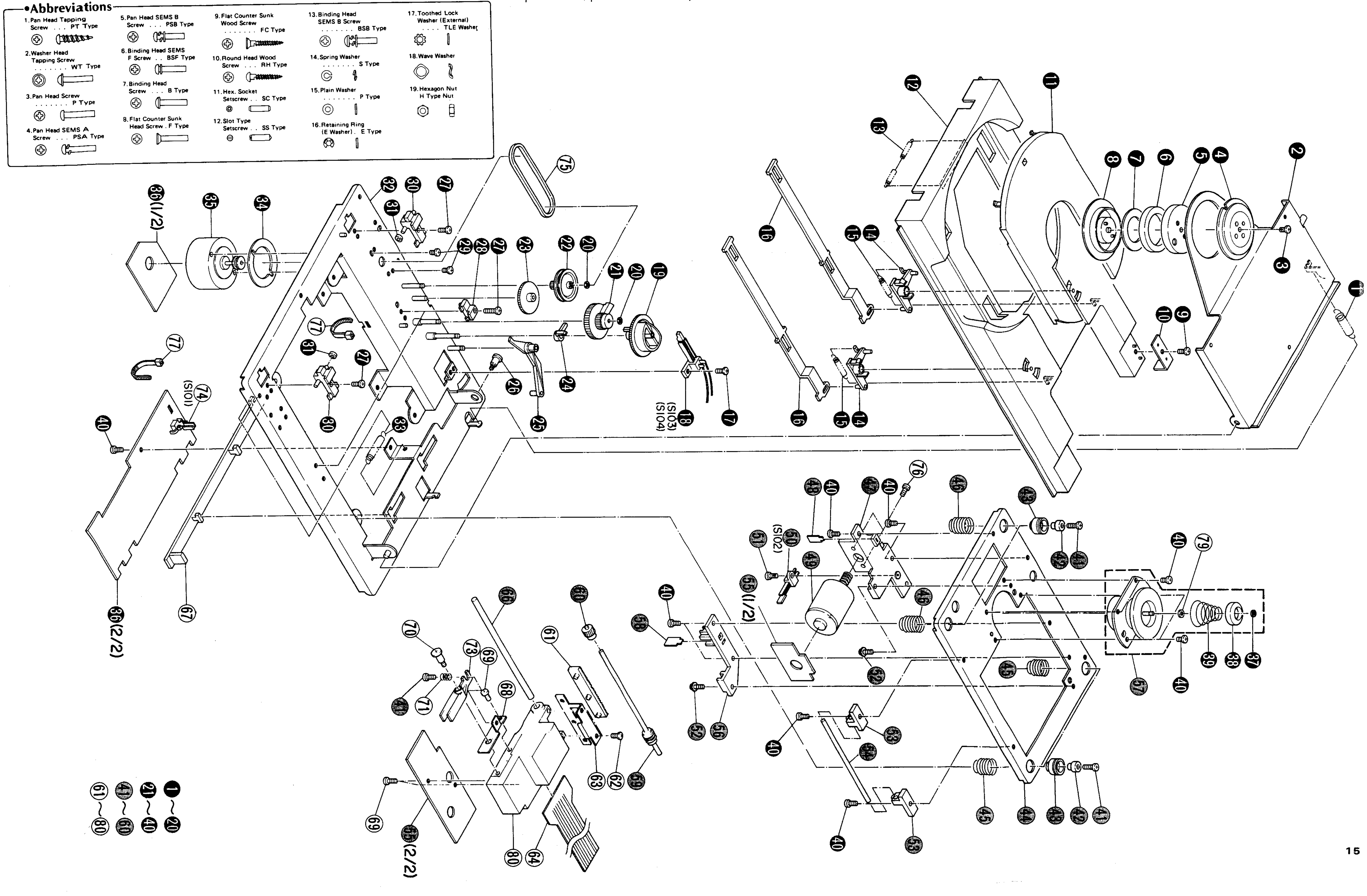
Parts No.	Stock No.	Description
101	58034900	Screw Caution
102	58028400	Panel Tray
103	58030300	Front Panel Ass'y (Black Model)
	58030400	Front Panel Ass'y (Silver Model)
103-1	58074300	Panel Mold-Deco
103-2	58029900	Eject Knob
103-3	58029500	Plastic RIVET
103-4	58074800	Screw, 2.6×8 B Type
103-5	58074600	Knob-3-PAUSE (Black Model)
	58075100	Knob-3-PAUSE (Silver Model)
103-6	58074700	Knob-3-PLAY (Black Model)
	58075000	Knob-3-PLAY (Silver Model)
103-7	58074800	Screw, 2.6×8 B Type
104	47747100	Knob, Power SW. (Black Model)
	47747000	Knob, Power SW. (Silver Model)
105	58029800	Joint-Knob-Power
106	58029700	Rod
107	58029600	Joint, 2.5
108	58034700	Screw-Pick (Transit Screw)
⚠ 109	58029401	Power Transformer (XX)
⚠	58029402	Power Transformer (UL, CSA)
⚠	58029405	Power Transformer (EU)
⚠	58029406	Power Transformer (BS)
110	58074900	Foot
111	58075400	Case, Power SW.
⚠ 112	58031600	Power Switch
113	58028500	Cover, Power SW.
114	58029500	Plastic Rivet, 3×5.5
115	58028700	Knob-MEMORY
116	58030000	Spring, Space
117	58028600	Knob, Space
⚠ 118	58030100	Cord Bush
⚠ 119	58029100	Power Supply Cord (BS)
⚠	58029200	Power Supply Cord (EU)
⚠	58029300	Power Supply Cord (CSA, UL)
⚠	58075300	Power Supply Cord (XX)
120	58031200	2P Output Terminal
121	58028100	Bonnet (Black Model)
	58028200	Bonnet (Silver Model)
⚠ 122	58075200	AC Inlet, Socket (XX)

5-1. Exploded View of Mechanism

- Though every part included in mechanism ass'y is numbered in exploded view, parts unlisted in the parts list are not supplied.

•Abbreviations

1. Pan Head Tapping Screw . . . PT Type
2. Washer Head Tapping Screw . . . . WT Type
3. Pan Head Screw . . . . P Type
4. Pan Head SEMS A Screw . . . PSA Type
5. Pan Head SEMS B Screw . . . PSB Type
6. Binding Head SEMS F Screw . . BSF Type
7. Binding Head Screw . . . B Type
8. Flat Counter Sunk Head Screw . F Type
9. Flat Counter Sunk Wood Screw . . . . FC Type
10. Round Head Wood Screw . . . RH Type
11. Hex. Socket Setscrew . . SC Type
12. Slot Type Setscrew . . SS Type
13. Binding Head SEMS B Screw . . . . BSB Type
14. Spring Washer . . . . S Type
15. Plain Washer . . . . P Type
16. Retaining Ring (E Washer) . E Type
17. Toothed Lock Washer (External) . . . . TLE Washer
18. Wave Washer
19. Hexagon Nut H Type Nut


1
2
3
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7
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9
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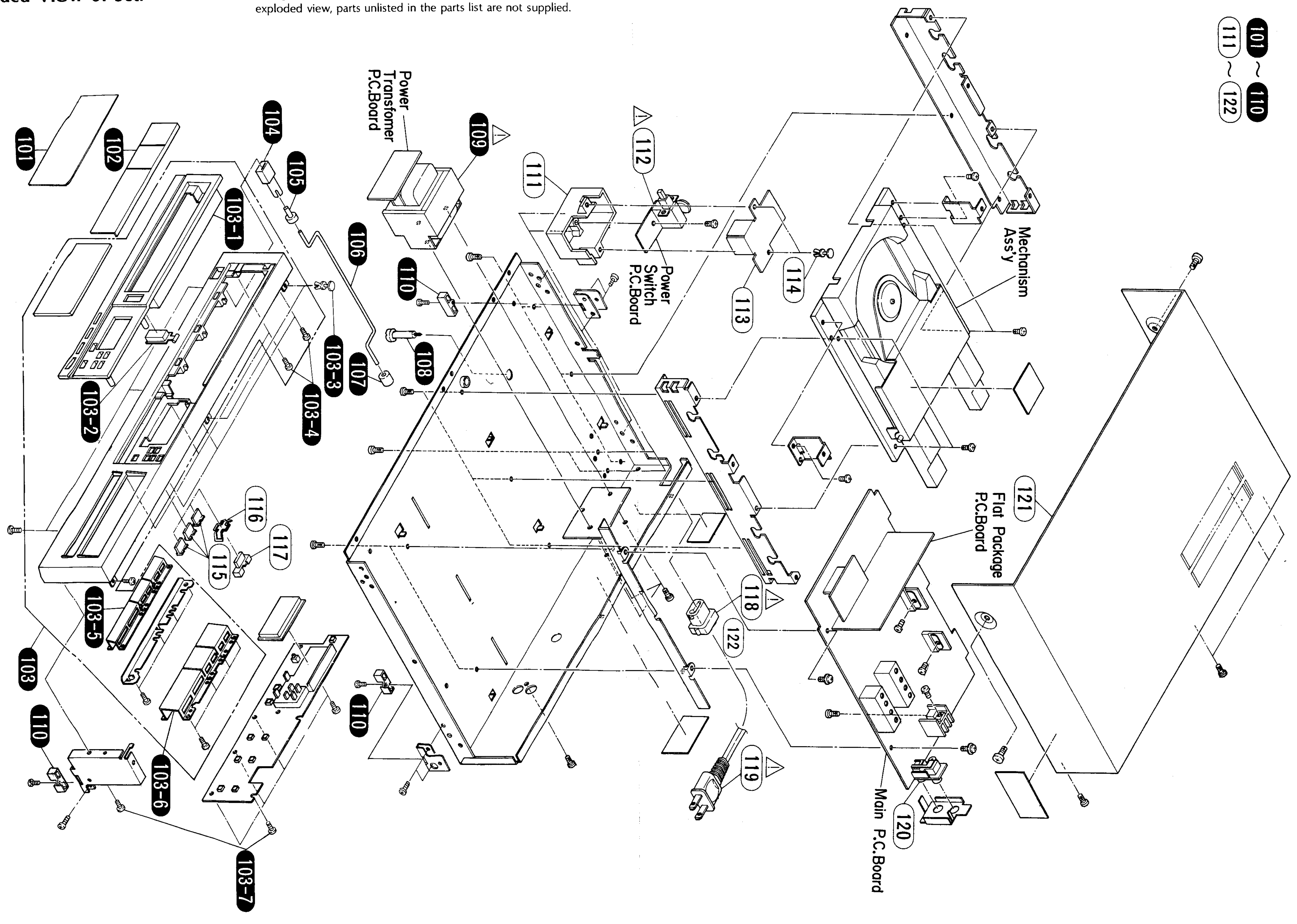
11
12
13
14
15
16
17
18
(S103)
(S104)
19
20
21
22
23
24
25
26
27
28
29
30
31
32
33
34
35
36(1/2)
36(2/2)
37
38
39
40
41
42
43
44
45
46
47
48
49
50
(S102)
51
52
53
54
55(1/2)
55(2/2)
56
57
58
59
60
61
62
63
64
65
66
67
68
69
70
71
72
73
74
(S101)
75
76
77
78
79
80
1~20
21~40
41~60
61~80

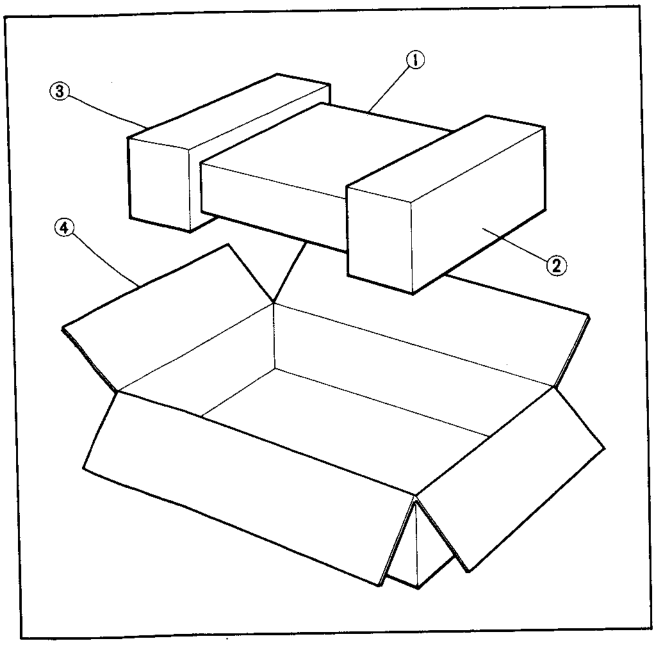
5-2. Exploded View of Set.

- Though every part included in mechanism ass'y is numbered in exploded view, parts unlisted in the parts list are not supplied.


101 ~ 110
111 ~ 122
101
102
103-1
104
105
106
Power Transfomer P.C.Board
109
110
108
107
103-3
103-4
103-2
111
112
Power Switch P.C.Board
113
114
Mechanism Ass'y
116
115
117
103-5
103
110
103-6
103-7
110
118
122
119
120
Main P.C.Board
121
Flat Package P.C.Board

6. PACKING LIST

Parts No.	Stock No.	Description
1	58048300	Vinyl Bag
2	58048100	Styrofoam Packing (Front)
3	58048200	Styrofoam Packing (Back)
4	58047700	Carton Case (Black Model)
	58047800	Carton Case (Silver Model)



7. ACCESSORY LIST

Parts No.	Stock No.	Description
	46984900	Operating Instruction
	58048600	Pin Plug Cord
	58075300	Power Supply Cord (XX)
	58079800	Mini Pin Plug Cord

8. PARTS LOCATION & PARTS LIST

8-1. Main PC Board (Stock No. 58079701)

Parts List

Parts No.	Stock No.	Description
● Transistor		
Q505, 506 707, 724	58031700	2SK30A
Q507, 508 702, 703 706, 710 721~723	46118801	2SC2878B
Q509, 604 726	07194701	2SA1015GR
Q510, 603 717, 718	58034000	2SC1815
Q708, 716	07194701	2SA1015
Q725, 901 904, 905	58031800	2SK365-BL
Q902, 906 908	58032300	2SD1413
Q903, 907	58032000	2SA473
● IC		
Q501	58032700	TD6705AP
Q502	58078800	μPD4053BC
Q503	58033200	NJM072D-E
Q504	58078900	NJM5532D-D
Q601	58040400	TMP-4740N-5942
Q602	58032900	TA7354P
Q605	58033300	PST520D
Q704, 719	58032800	TA7256P
Q705, 714 720	58033000	TA75458S
Q711~713	46428900	TC40H004P
Q715	07107500	TC4013BP
● Diode		
D501~505 601~607, 701~708, 711	58031500	1SS176
D709	46102500	05Z 8.2Y
D710	46102600	05Z 8.2Z
⚠ D901, 902	58032500	1B4B41
D903	46101600	05Z 6.2Y
D904	46101300	05Z 5.6Y
D905, 906	46102800	05Z 9.1Y
D907	46102200	05Z 7.5Y
Z301	58033500	Xtal
R601, 602	58079300	5.6kΩ ×6, A.R.
R820	58079400	10Ω 1W, M.R.
R507	58033800	10kΩ S.V.R. offset
R508	58033800	10kΩ S.V.R. offset
R705	58033800	10kΩ S.V.R. focus gain
R727	58033800	10kΩ S.V.R. TC gain
⚠ R901~904	00120000	1Ω 1/2W F.R.
⚠ C901	58079100	4700pF 400V C.C. (UL,CSA,AS)
⚠	58079200	4700pF 400V C.C. (XX,.EU,BS)
L401	58033600	Coil RT72-5445
	58033700	Coil RT71S5127

8-2. Display PC Board (Stock No. 58033900)

Parts List

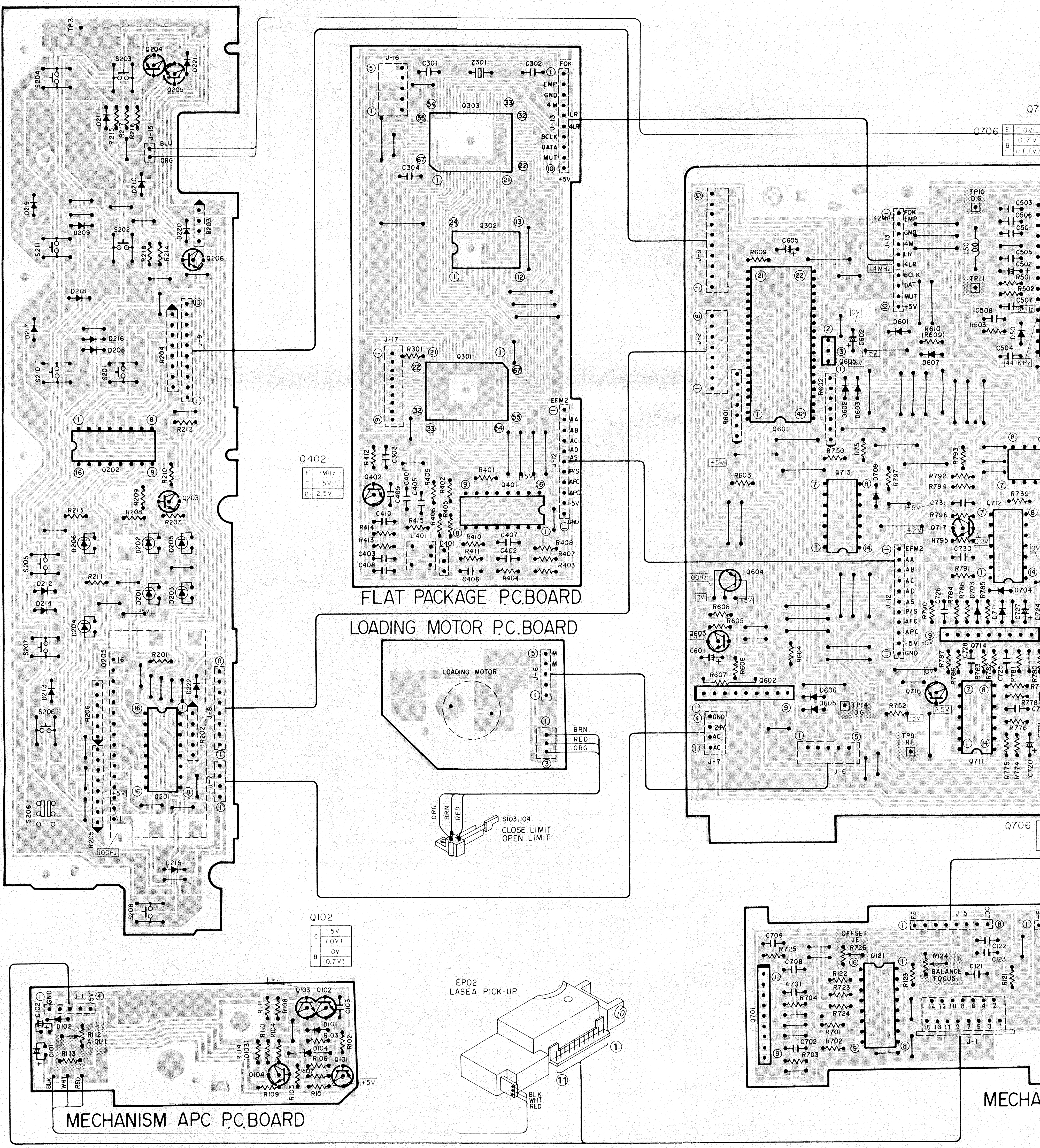
Parts No.	Stock No.	Description
● Transistor		
Q203, 205 206	58034000	2SC1815
Q204	07194701	2SA1015
● IC		
Q201	07197300	TC5066BP
Q202	58034200	TC5067BP
● Diode		
D208~222	58031500	1SS176
● LED		
D201~206	58034100	TLS-208
Q205	58034400	Display Tube, FG-48E
R202	58077600	5.6kΩ ×4, A.R.
R203	58077700	47kΩ ×3, A.R.
R204	58077800	47kΩ ×7, A.R.
R205	58077900	56kΩ ×5, A.R.
R206	58078000	56kΩ ×5, A.R.
S201~208 210, 211	58034500	Tact SW.
S209	58074200	Push SW., Auto Spacing

8-3. Flat Package P.C. Board (Stock No. 58078100)

Parts List

Parts No.	Stock No.	Description
● Transistor		
Q402	07273601	2SC1923
● IC		
Q301	58030800	TC9178AF
Q302	58031000	TC5516AF
Q303	58030900	TC9179F
Q401	58032600	TD6315BP
● Diode		
D401	58032400	1SV147
L401	58033600	Coil-RT72-5445
Z301	58033500	Xtal

• PARTS LOCATION


FLAT PACKAGE P.C.BOARD
LOADING MOTOR P.C.BOARD
LOADING MOTOR
MECHANISM APC P.C.BOARD
MECHA
EP02
LASEA PICK-UP
S103,104
CLOSE LIMIT
OPEN LIMIT
BRN
RED
ORG
BLK
WHT
RED
BLU
ORG
Q402
E 17MHz
C 5V
B 2.5V
Q102
C 5V (0V)
B 0V (0.7V)
Q706
OFFSET TE
BALANCE FOCUS
A-OUT
Q303
Q302
Q301
Q401
Q601
Q201
Q202
Q121
J-1
J-5
J-6
J-7
J-8
J-9
J-12
J-13
J-15
J-16
J-17
FOK
EMP
GND
4M
LR
4LR
BCLK
DATA
MUT
+5V
EFM2
AA
AB
AC
AD
AS
P/S
AFC
APC
-5V
GND
TP9
TP10
TP11
TP14
100Hz
4.2kHz
44.1kHz
1.4MHz
4.2MHz

8-4. Mechanism APC PC Board
(Stock No. 58078500)

Parts List

Parts No.	Stock No.	Description
● Transistor		
Q101	58078600	2SA966
Q102	58034000	2SC1815
Q103	58034000	2SC1815
Q104	58034000	2SC1815
● Diode		
D101	58031500	1SS176
D102	58031500	1SS176
● Zener Diode		
D104	46099500	05Z 3.3Y
R112	58078700	10kΩ, S.V.R., LPC

8-5. Mechanism PC Board (Stock No. 58078200)

Parts List

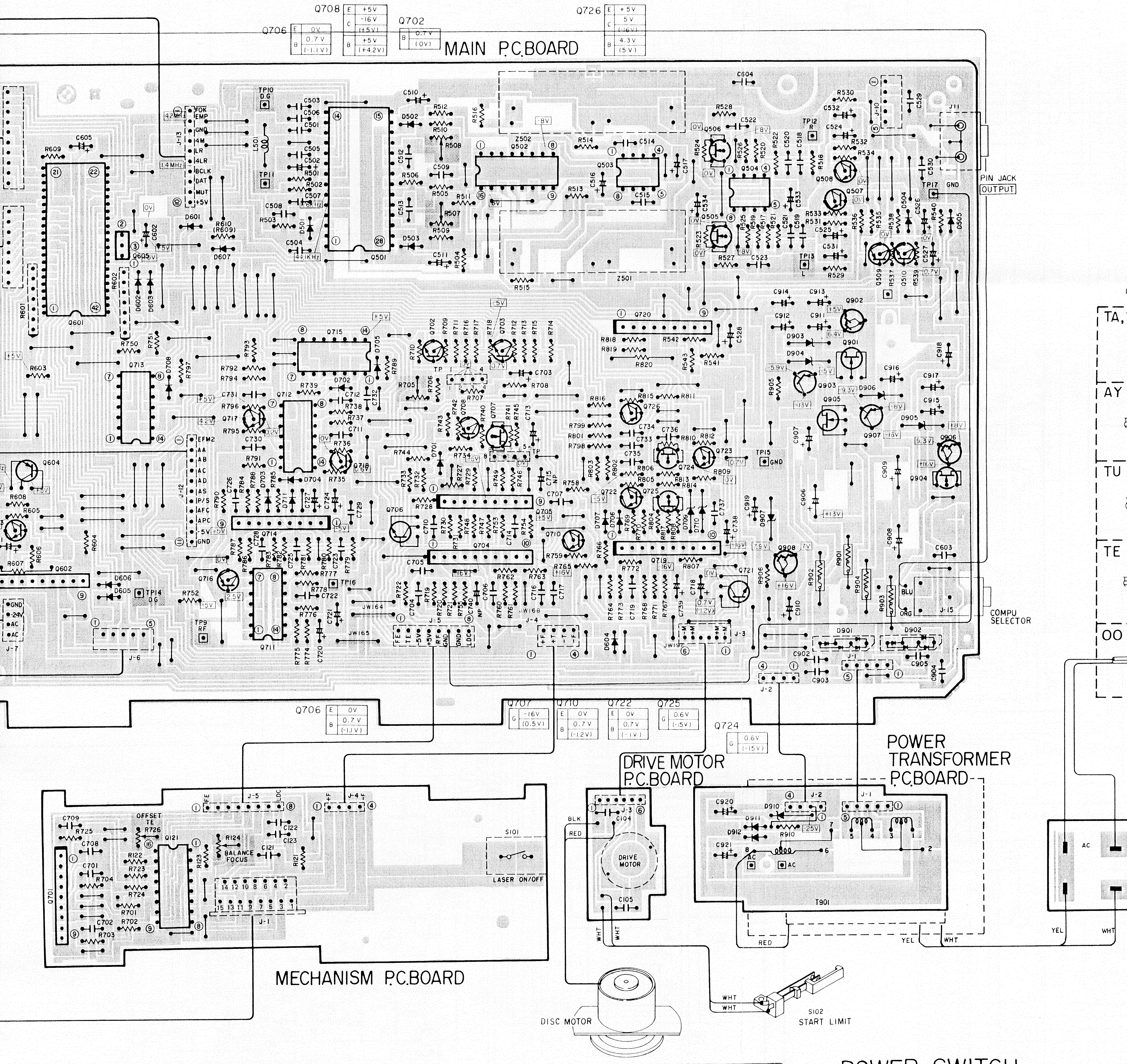
Parts No.	Stock No.	Description
● IC		
Q121	58078300	TA7779P
Q701	58033000	TA75458S
R124	58078400	20kΩ, S.V.R. FOCUS BALANCE
R726	58078400	20kΩ, S.V.R. TE OFFSET
S101	58077300	Leaf SW., Laser ON/OFF

8-6. Power Transformer PC Board

Parts List

Parts No.	Stock No.	Description
● Diode		
D911	58031500	1SS176
D912	58031500	1SS176
● Zener Diode		
D910	58031400	05Z 24Y

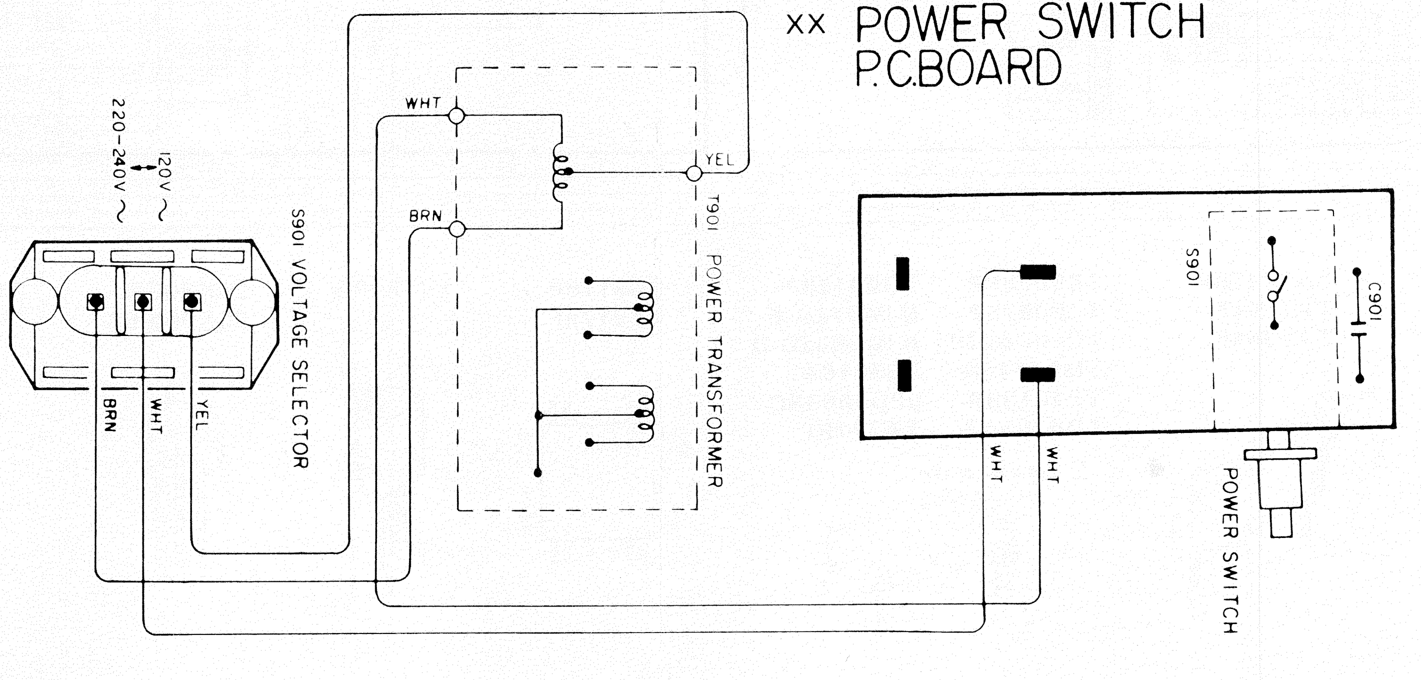
※ The voltage values are measured without disc when power is ON
The voltage values included in ( ) are measured at PLAY mode


MAIN P.C.BOARD
Q708 E +5V C -16V (+5V) B +5V (+4.2V)
Q702 0.7V (0V)
Q706 E 0V B 0.7V (-1.1V)
Q726 E +5V C 5V (-16V) B 4.3V (5V)
PIN JACK OUTPUT
COMPU SELECTOR
Q707 G -16V (0.5V)
Q710 E 0V B 0.7V (-1.2V)
Q722 E 0V B 0.7V (-1V)
Q725 G 0.6V (-15V)
Q724 G 0.6V (-15V)
DRIVE MOTOR P.C.BOARD
DRIVE MOTOR
POWER TRANSFORMER P.C.BOARD
T901
MECHANISM P.C.BOARD
OFFSET TE
BALANCE FOCUS
S101
LASER ON/OFF
DISC MOTOR
S102 START LIMIT
BLK
RED
WHT
YEL

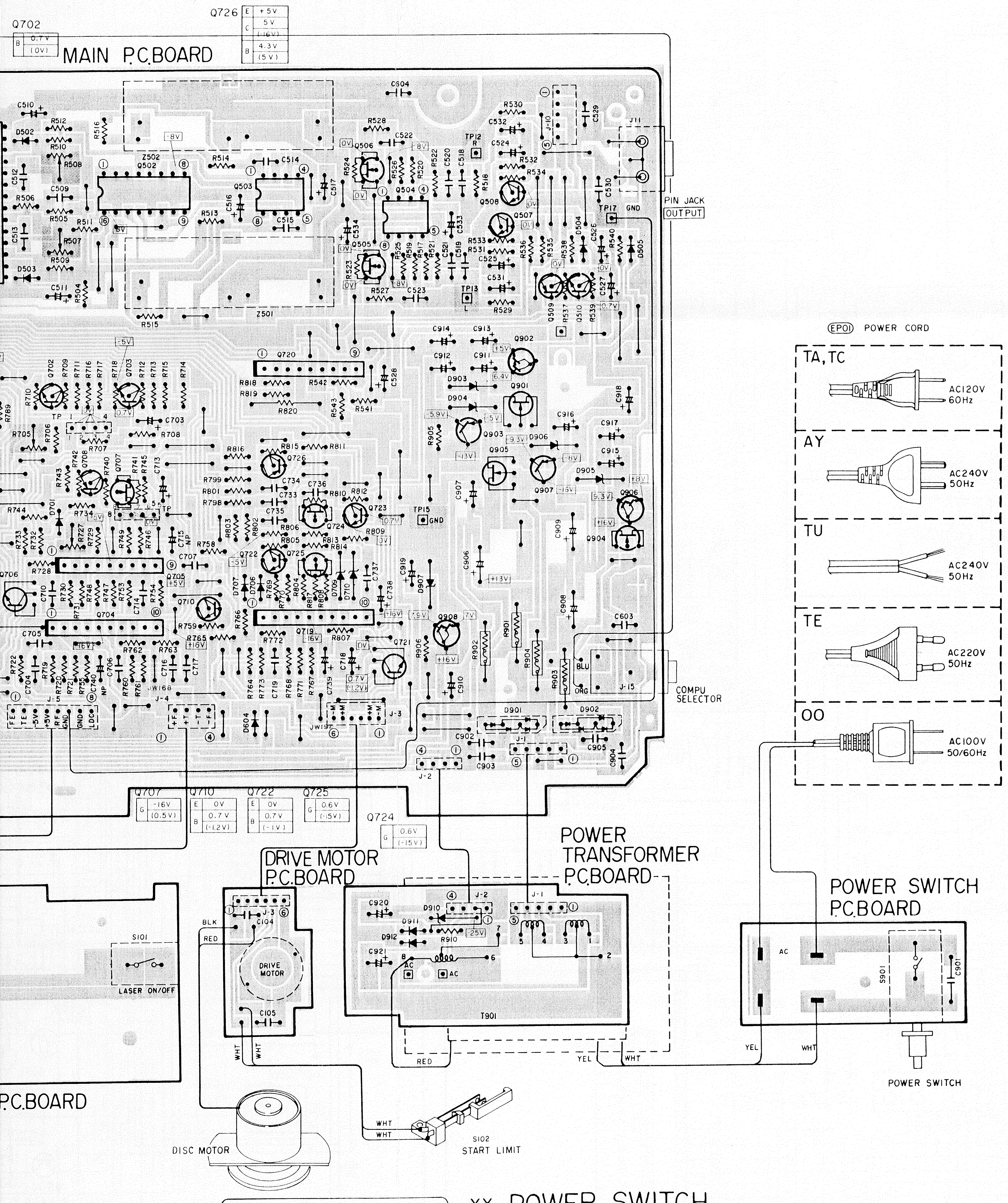
Power Transformer PC Board

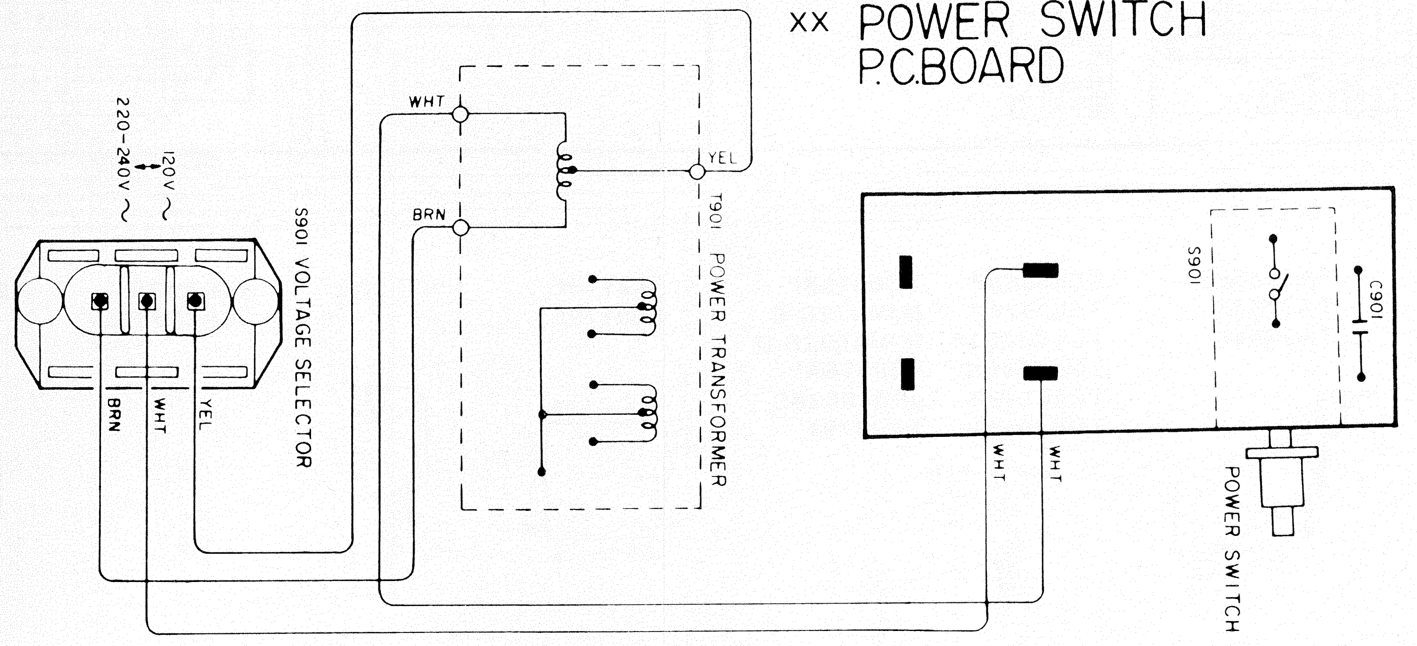
s List

s No.	Stock No.	Description
ode		
911	58031500	1SS176
912	58031500	1SS176
ener Diode		
910	58031400	05Z 24Y

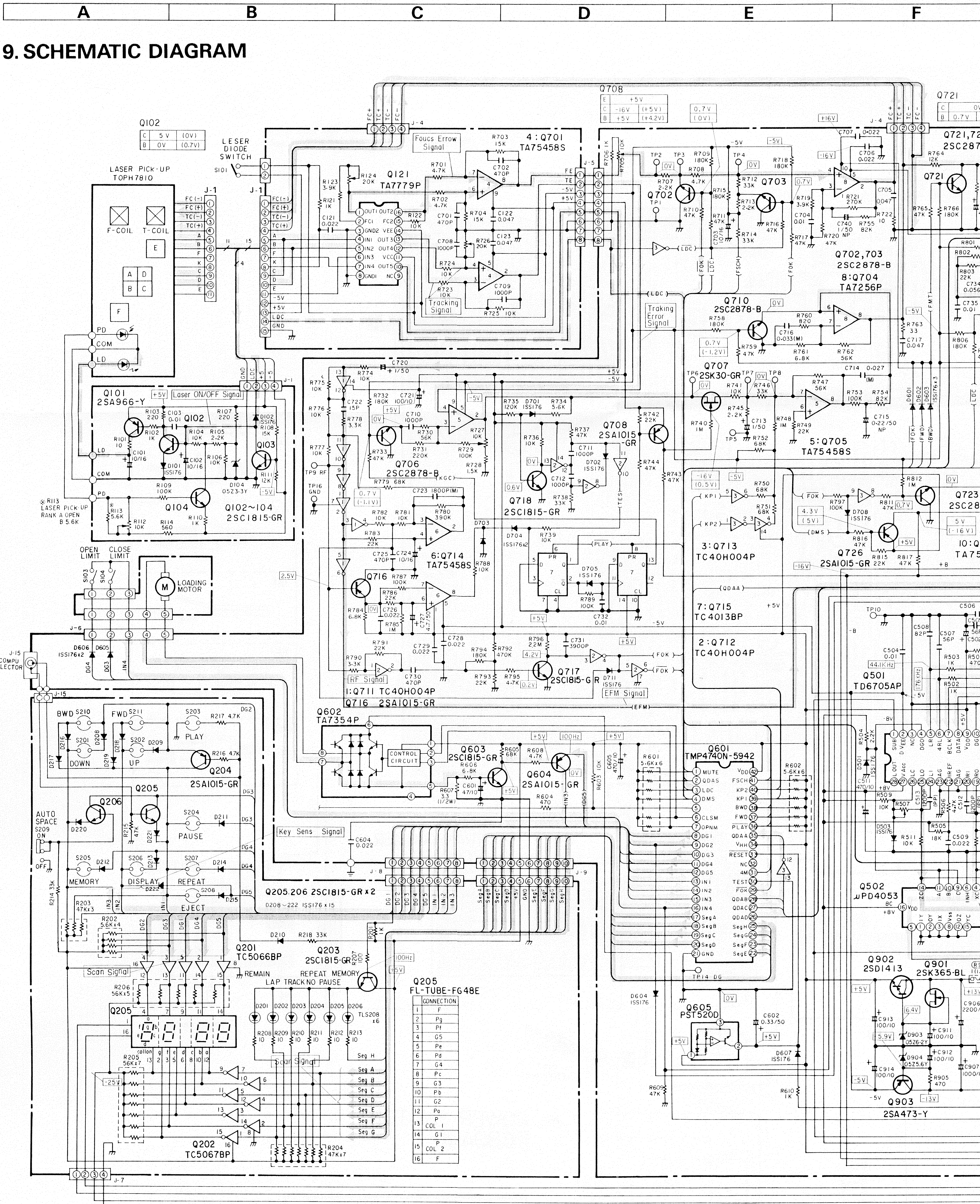

xx POWER SWITCH P.C.BOARD
220-240V ~
120V ~
S901 VOLTAGE SELECTOR
BRN
WHT
YEL
T901 POWER TRANSFORMER
S901
C901
POWER SWITCH

※ The voltage values are measured without disc when power is ON.
The voltage values included in ( ) are measured at PLAY mode.

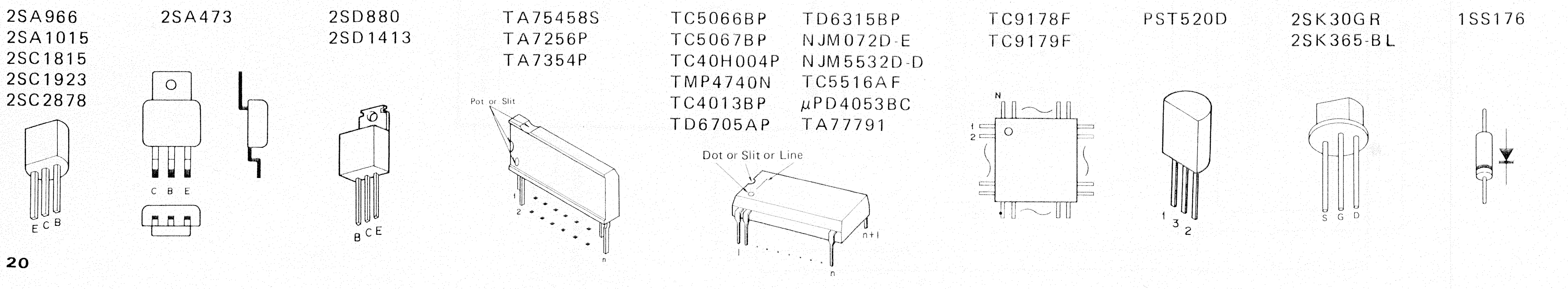

MAIN P.C.BOARD
Q702
Q726
PIN JACK
OUTPUT
COMPU SELECTOR
Q707
Q710
Q722
Q725
Q724
DRIVE MOTOR P.C.BOARD
POWER TRANSFORMER P.C.BOARD
T901
DRIVE MOTOR
S101
LASER ON/OFF
P.C.BOARD
DISC MOTOR
S102
START LIMIT
EP01 POWER CORD
TA, TC
AC120V 60Hz
AY
AC240V 50Hz
TU
AC240V 50Hz
TE
AC220V 50Hz
OO
AC100V 50/60Hz
POWER SWITCH P.C.BOARD
S901
C901
POWER SWITCH
YEL
WHT
RED
BLK
BRN


xx POWER SWITCH P.C.BOARD
220-240V ~
120V ~
S901 VOLTAGE SELECTOR
T901 POWER TRANSFORMER
WHT
BRN
YEL
S901
C901
POWER SWITCH

9. SCHEMATIC DIAGRAM

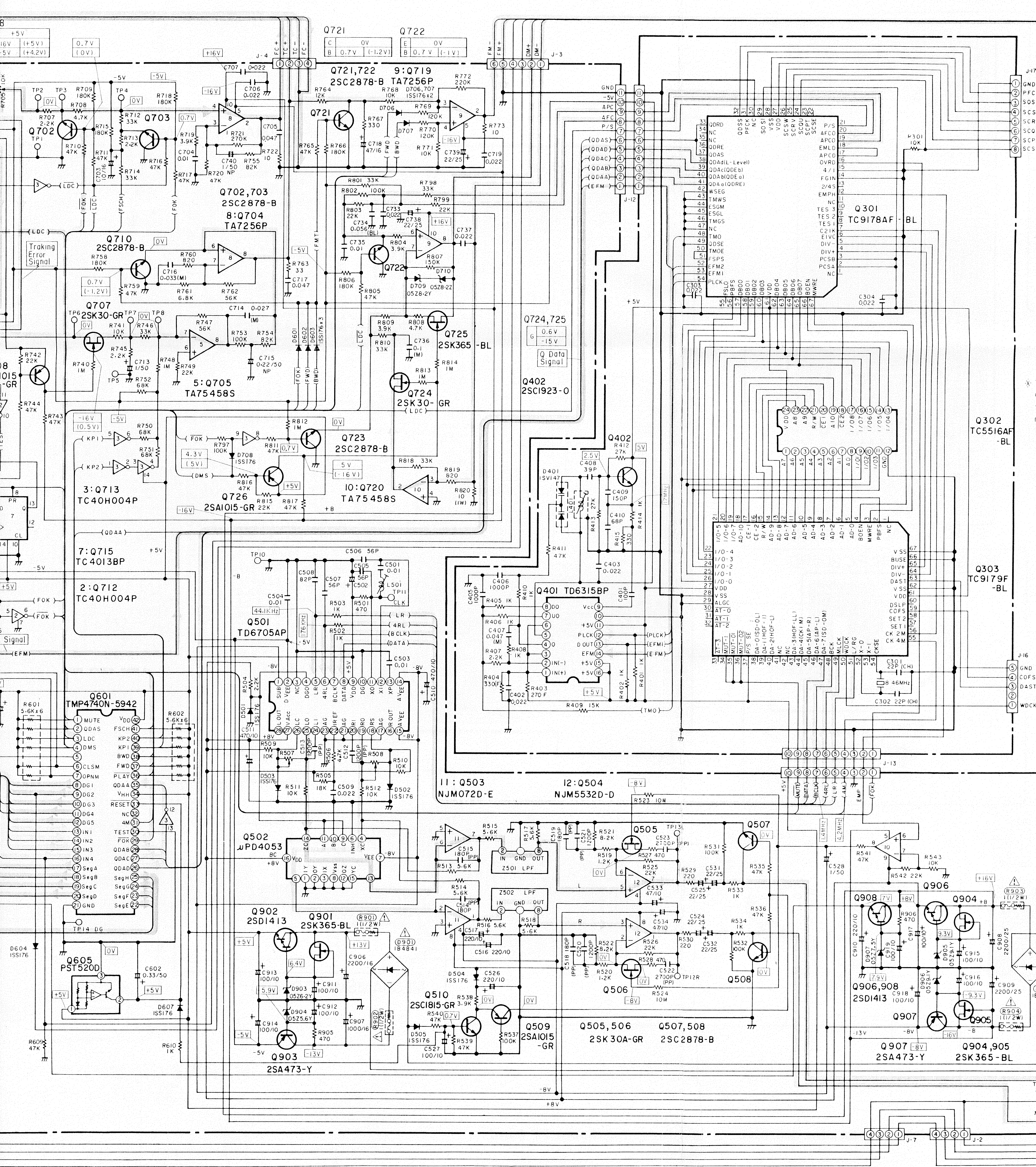

A
B
C
D
E
F
LASER PICK-UP TOPH7810
F-COIL
T-COIL
PD
COM
LD
LESER DIODE SWITCH
S101
J-1
Q102
Q121 TA7779P
4:Q701 TA75458S
Foucs Errow Signal
Tracking Signal
Traking Error Signal
Q708
Q721
Q721,722 2SC2878
Q702 Q703
Q702,703 2SC2878-B
8:Q704 TA7256P
Q710 2SC2878-B
Q707 2SK30-GR
5:Q705 TA75458S
Q101 2SA966-Y
Laser ON/OFF Signal
Q102~104 2SC1815-GR
Q104
Q103
※R113 LASER PICK-UP RANK A OPEN B 5.6K
Q706 2SC2878-B
6:Q714 TA75458S
Q716
Q708 2SA1015-GR
Q718 2SC1815-GR
3:Q713 TC40H004P
Q723 2SC2878
Q726 2SA1015-GR
10:Q TA75
7:Q715 TC4013BP
2:Q712 TC40H004P
Q717 2SC1815-GR
RF Signal
EFM Signal
1:Q711 TC40H004P
Q716 2SA1015-GR
OPEN LIMIT
CLOSE LIMIT
LOADING MOTOR
J-15 COMPU SELECTOR
Q602 TA7354P
CONTROL CIRCUIT
Q603 2SC1815-GR
Q604 2SA1015-GR
Q601 TMP4740N-5942
Q501 TD6705AP
Q502 μPD4053
BWD S210
FWD S211
DOWN
UP
S203 PLAY
Q204 2SA1015-GR
Q205
Q206
AUTO SPACE S209 ON OFF
S204 PAUSE
MEMORY
DISPLAY
REPEAT
EJECT
Key Sens Signal
Q205.206 2SC1815-GR×2
D208~222 1SS176×15
Q201 TC5066BP
Q203 2SC1815-GR
Scan Signal
REMAIN
LAP TRACK NO PAUSE
REPEAT MEMORY
Q205 FL-TUBE-FG48E
CONNECTION
Q202 TC5067BP
TLS208 ×6
Q605 PST520D
Q902 2SD1413
Q901 2SK365-BL
Q903 2SA473-Y
J-4
J-5
J-6
J-7
J-8
J-9

	CONNECTION
1	F
2	Pg
3	Pf
4	G5
5	Pe
6	Pd
7	G4
8	Pc
9	G3
10	Pb
11	G2
12	Pa
13	P COL 1
14	G1
15	P COL 2
16	F

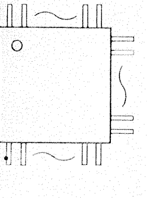

2SA966
2SA1015
2SC1815
2SC1923
2SC2878
E C B
2SA473
C B E
2SD880
2SD1413
B C E
TA75458S
TA7256P
TA7354P
Pot or Slit
TC5066BP
TC5067BP
TC40H004P
TMP4740N
TC4013BP
TD6705AP
TD6315BP
NJM072D-E
NJM5532D-D
TC5516AF
μPD4053BC
TA7779I
Dot or Slit or Line
TC9178F
TC9179F
N
PST520D
1 3 2
2SK30GR
2SK365-BL
S G D
1SS176

E F G H I J

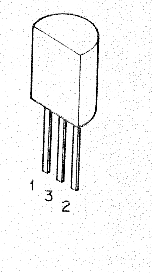
- Design and specifications subject
- La présention et les spécifications
tes d'améliorations éventuelles.
- Änderungen, die dem technischen


Q721 Q722
Q721,722 2SC2878-B 9:Q719 TA7256P
Q703
Q702
Q702,703 2SC2878-B
8:Q704 TA7256P
Q710 2SC2878-B
Traking Error Signal
Q707 2SK30-GR
5:Q705 TA75458S
3:Q713 TC40H004P
7:Q715 TC4013BP
2:Q712 TC40H004P
Q723 2SC2878-B
Q726 2SA1015-GR
10:Q720 TA75458S
Q722
Q725 2SK365-BL
Q724 2SK30-GR
Q724,725
Q Data Signal
Q402 2SC1923-O
Q301 TC9178AF-BL
Q302 TC5516AF-BL
Q303 TC9179F-BL
Q401 TD6315BP
Q501 TD6705AP
Q601 TMP4740N-5942
Q502 µPD4053
11:Q503 NJM072D-E
12:Q504 NJM5532D-D
Z501 LPF
Z502 LPF
Q505 Q506 Q507 Q508
Q505,506 2SK30A-GR
Q507,508 2SC2878-B
Q509 2SA1015-GR
Q510 2SC1815-GR
Q605 PST520D
Q902 2SD1413
Q901 2SK365-BL
Q903 2SA473-Y
D901 1B4B41
Q906,908 2SD1413
Q907 2SA473-Y
Q904,905 2SK365-BL
J-2 J-3 J-4 J-7 J-12 J-13 J-16 J-17

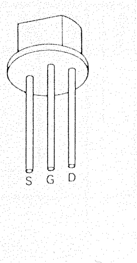
C9178F
C9179F



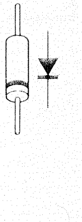
PST520D



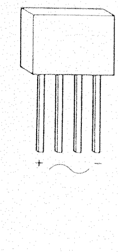
2SK30GR
2SK365-BL



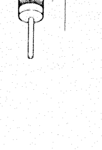
1SS176



1B4B41



05Z3.3Y 05Z8.2Y
05Z5.6Y 05Z9.1Y
05Z6.2Y 05Z24
05Z7.5Y

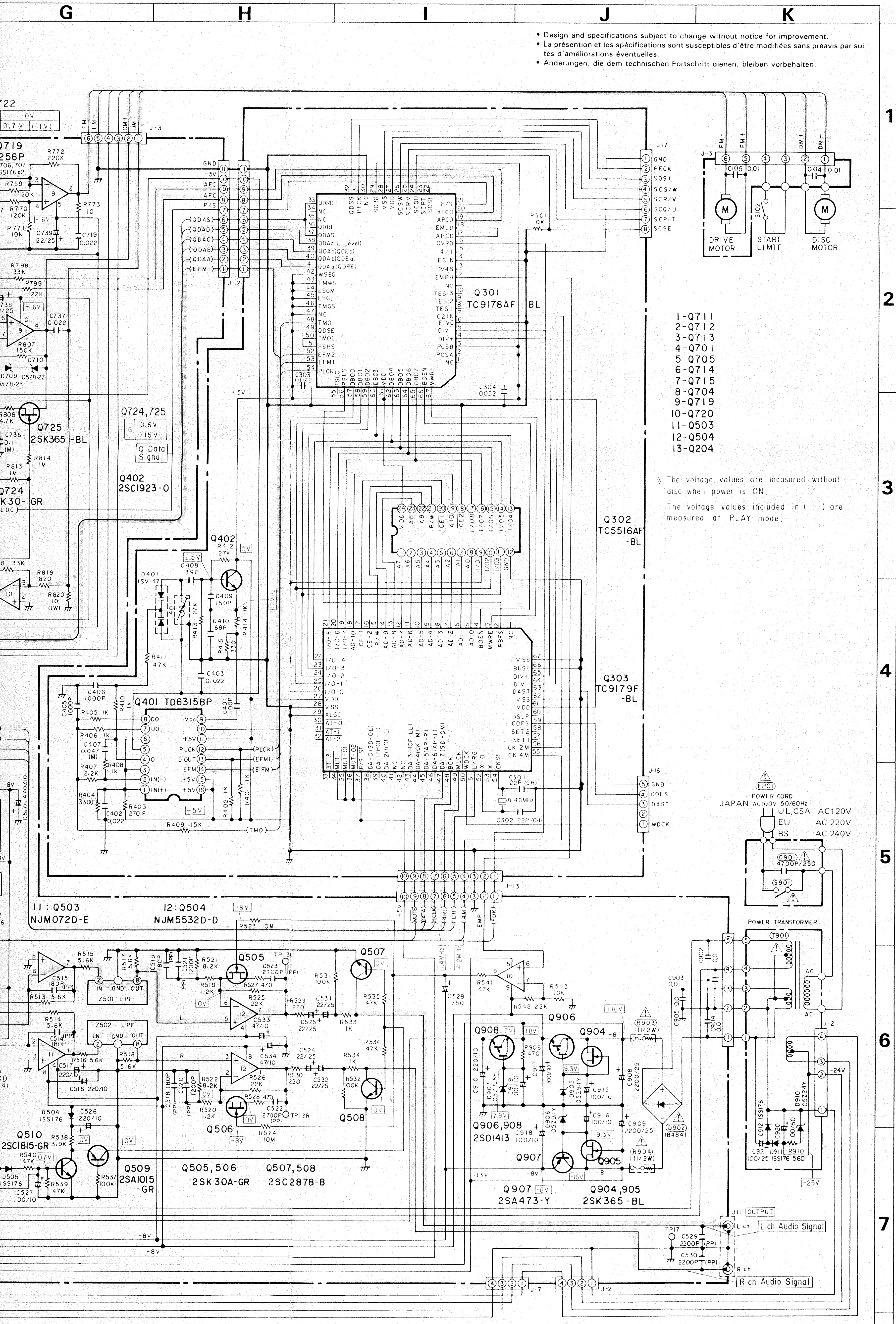


The voltages are measured as STOP mode.
All voltages are measured with a 10MΩ/DC electric volt meter.

⚠ is Safety Part.
Use only replacement parts recommended by the manufacturer.

Schematic diagram is subject to change without notice.

- Design and specifications subject to change without notice for improvement.
- La présention et les spécifications sont susceptibles d'être modifiées sans préavis par suites d'améliorations éventuelles.
- Änderungen, die dem technischen Fortschritt dienen, bleiben vorbehalten.


G
H
I
J
K
1
2
3
4
5
6
7
8
J-3
FM−
FM+
DM+
DM−
Q719
256P
R772 220K
R769
R770 120K
R771 10K
C739 22/25
C719 0.022
R773 10
R798 33K
R799 22K
C737 0.022
R807 150K
D710
D709 05Z8.2Y
Q725 2SK365-BL
Q724,725
0.6V
-15V
Q Data Signal
R814 1M
R813 1M
Q724
2SK30-GR
Q402 2SC1923-O
R819 820
R820 10 (1W)
J-12
GND
−5V
APC
AFC
P/S
QDAS
QDAD
QDAC
QDAB
QDAA
EFM
J-17
GND
PFCK
SOSI
SCS/W
SCR/V
SCQ/U
SCP/T
SCSE
R301 10K
Q301
TC9178AF-BL
C303 0.022
C304 0.022
+5V
C105 0.01
C104 0.01
S102
DRIVE MOTOR
START LIMIT
DISC MOTOR
1-Q711
2-Q712
3-Q713
4-Q701
5-Q705
6-Q714
7-Q715
8-Q704
9-Q719
10-Q720
11-Q503
12-Q504
13-Q204
Q302
TC5516AF-BL
Q402
R412 27K
C408 39P
D401 1SV147
L401
C409 150P
C410 68P
R413 27K
R414 1K
R415 330
R411 47K
C403 0.022
17MHz
Q303
TC9179F-BL
Q401 TD6315BP
C405 1000P
C406 1000P
R405 1K
R410 1K
R406 1K
C407 0.047 (M)
R407 2.2K
R408 1K
R404 330(F)
R403 270F
C402 0.022
R409 15K
R402 1K
R401 1K
C401 100P
PLCK
EFM
TMO
C301 22P (CH)
X301 8.46MHz
C302 22P (CH)
J-16
GND
COFS
DAST
WDCK
EP01
POWER CORD
JAPAN AC100V 50/60Hz
UL,CSA AC120V
EU AC 220V
BS AC 240V
C901 4700P/250
S901
J-13
MUTE
DATA
BCLK
LR
4M
EMP
FOK
11 : Q503
NJM072D-E
12 : Q504
NJM5532D-D
R523 10M
POWER TRANSFORMER
T901
AC
R515 5.6K
R517 5.6K
C519 180P
C521 1200P
R521 8.2K
Q505
TP13L
C523 2700P (PP)
R527 470
R519 1.2K
Q507
R531 100K
R535 47K
R525 22K
R529 220
C531 22/25
C525 22/25
R533 1K
C533 47/10
C515 180P
R513 5.6K
Z501 LPF
IN GND OUT
R514 5.6K
Z502 LPF
C514 180P
R516 5.6K
R518 5.6K
C517 220/10
C516 220/10
C518 180P
C520 1200P
R522 8.2K
R526 22K
R530 220
C534 47/10
C524 22/25
C532 22/25
R534 1K
R536 47K
R532 100K
Q508
R520 1.2K
R528 470
C522 2700P (PP)
TP12R
Q506
R524 10M
D504 1SS176
C526 220/10
Q510 2SC1815-GR
R538 3.9K
R540 47K
D505 1SS176
C527 100/10
R539 47K
R537 100K
Q509 2SA1015-GR
Q505,506 2SK30A-GR
Q507,508 2SC2878-B
C528 1/50
R541 47K
R543 10K
R542 22K
Q906
Q908
Q904
R906 470
C917 100/10
C910 220/10
D907 05Z7.5Y
C919 100/10
D905 05Z9.1Y
C915 100/10
C908 2200/25
D906 05Z9.1Y
C916 100/10
C909 2200/25
Q906,908 2SD1413
C918 100/10
Q907
Q905
R903 1 (1/2W)
R904 1 (1/2W)
D902 1B4B41
C902 0.01
C903 0.01
C905 0.01
C904 0.01
J-2
D912 1SS176
C920
D910 05Z24Y
C921 100/25
D911 1SS176
R910 560
Q907 2SA473-Y
Q904,905 2SK365-BL
J11 OUTPUT
L ch
L ch Audio Signal
R ch
R ch Audio Signal
TP17
C529 2200P (PP)
C530 2200P (PP)
J-7
J-2
−8V
+8V
−13V
+16V
−9.3V
9.3V
7.9V
−24V
−25V
0V
5V
2.5V
+5V
−8V

※ The voltage values are measured without disc when power is ON.

The voltage values included in ( ) are measured at PLAY mode.

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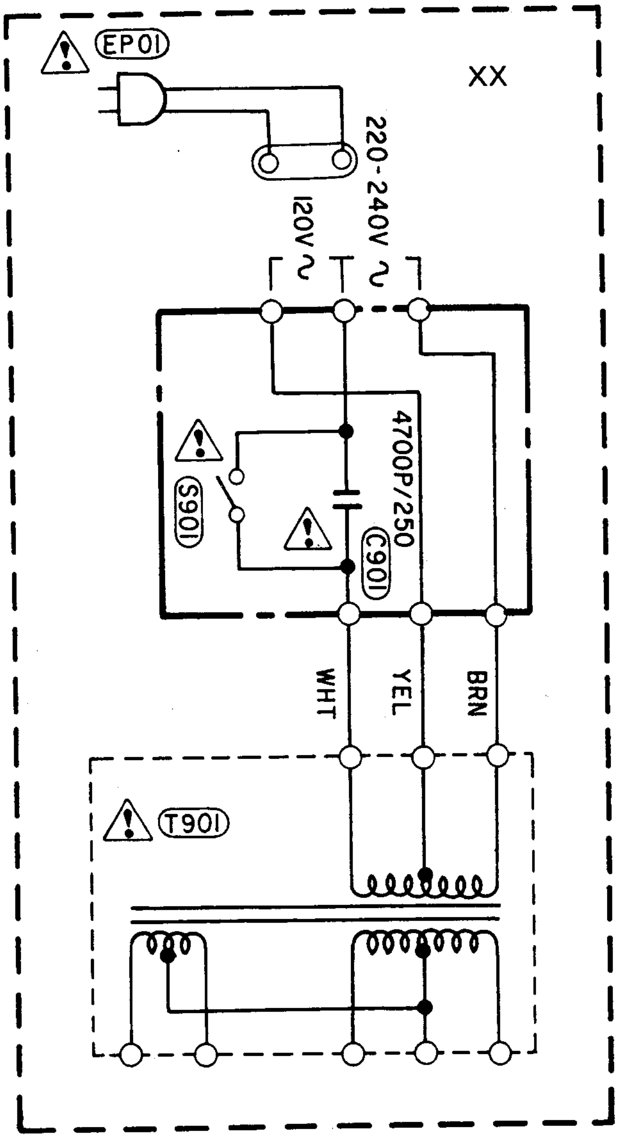
05Z3.3Y 05Z8.2Y
05Z5.6Y 05Z9.1Y
05Z6.2Y 05Z24
05Z7.5Y

The voltages are measured as STOP mode.
All voltages are measured with a 10MΩ/DC electric volt meter.

⚠ is Safety Part.
Use only replacement parts recommended by the manufacturer.

Schematic diagram is subject to change without notice.


EP01
XX
220-240V ∿
120V ∿
4700P/250
C901
S901
WHT
YEL
BRN
T901